KEK BPM (18K12) Status Report

2013/June/27

Ryo Ichimiya (KEK)

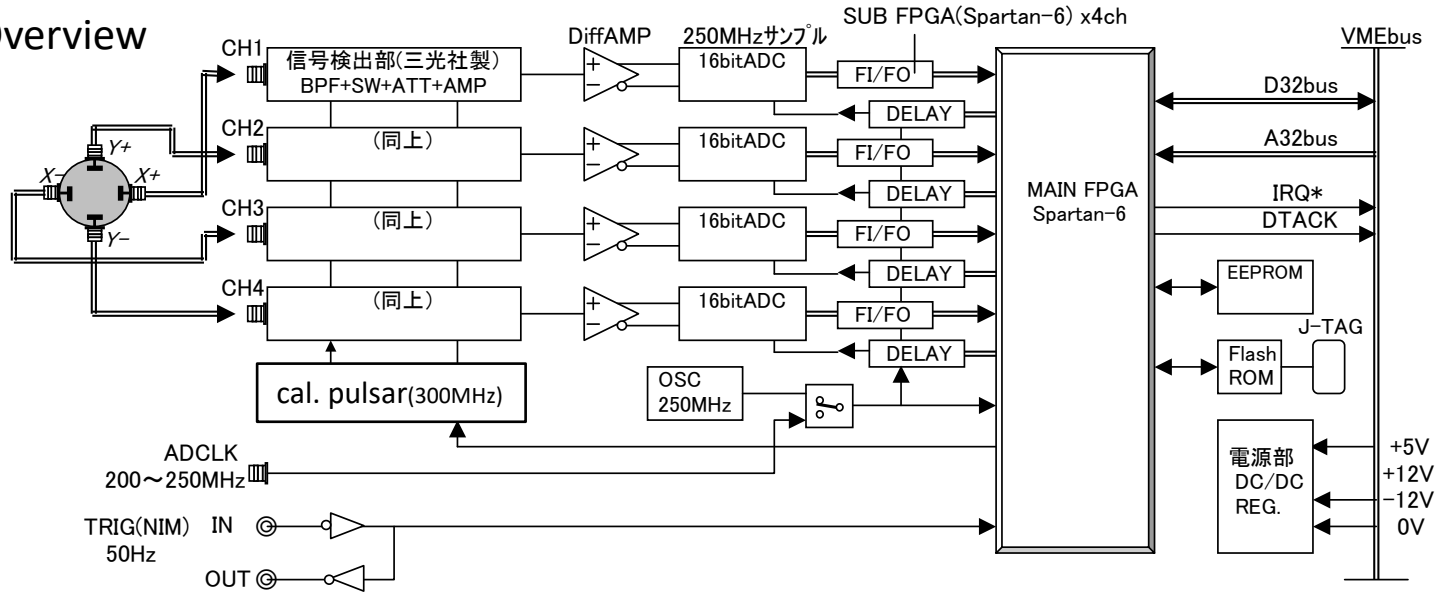
rev. 2.20（+Eng.）

Candidates to get worth position resolution

1. BPF, ADC input circuit may operate in non-linear region.
2. Tails of BPF output spectrum exceeds Nyquist window (250-375MHz) and it makes folding noise.
3. Triple harmonic (900MHz) also may cause folding noise.
4. Analogue noise from DC-DC converter etc. introduces GND wobble, EMI and so forth.

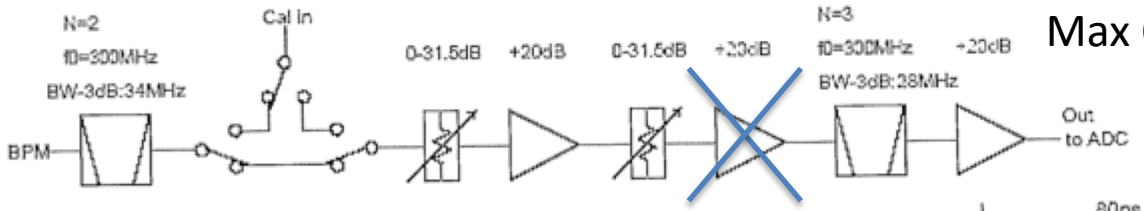
Block diagram

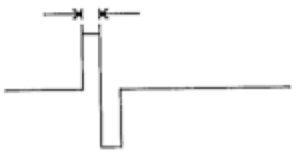
Overview



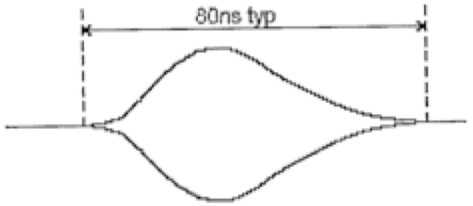
[specifications]
Gain: 32.5dB(confirmed)
Max Output: +12dBm
(2.5Vpp)

Analogue Frontend



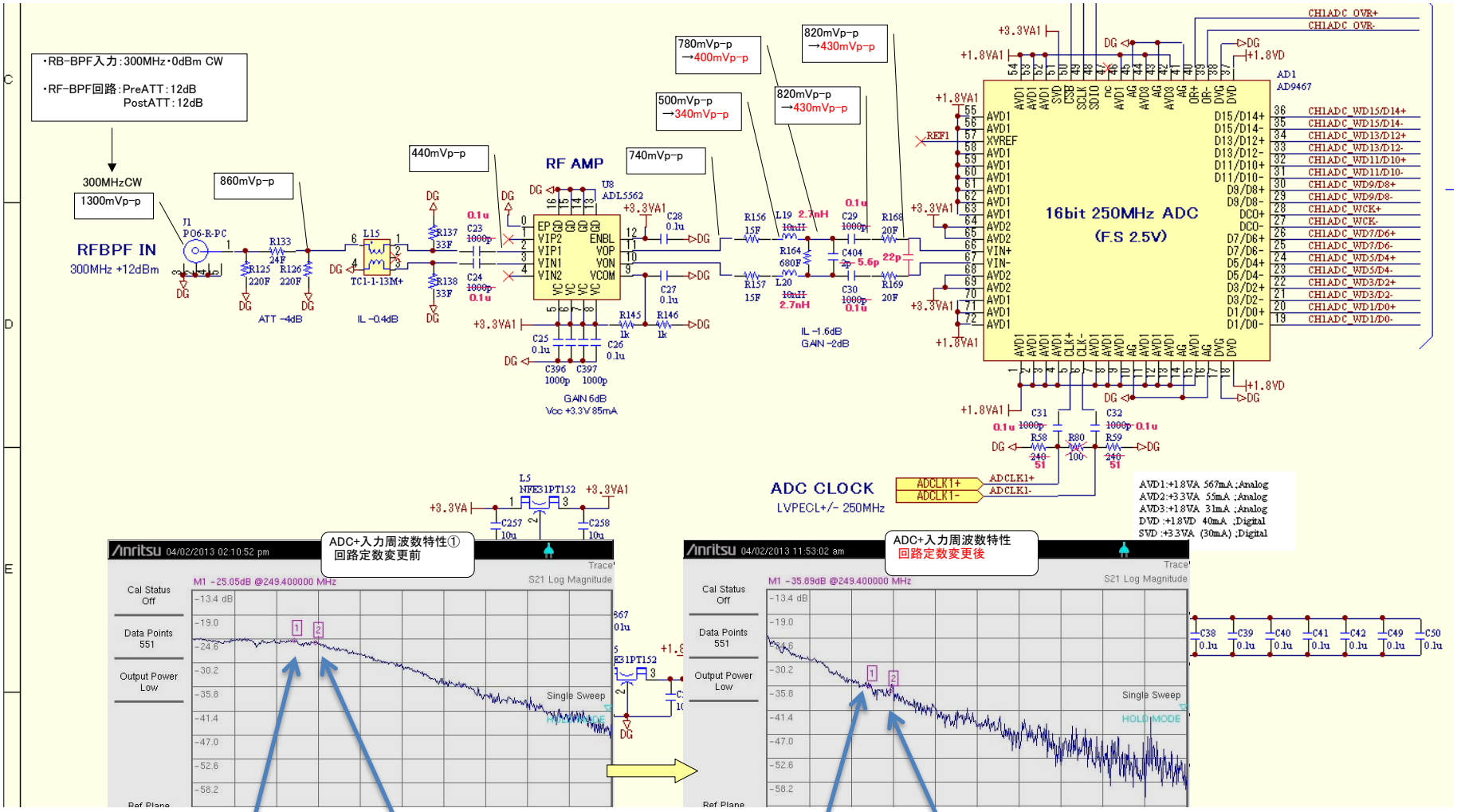


Att.(pre) Att.(post)
0-31.5dB 0-31.5dB



*These tests presented in this slide have been performed with Pre:8dB, Post:0dB setting. Total BPF gain is +24.5dB(x16.8).

ADC input circuit



22pF -> Snubber circuit

- Thanks to Adrew's suggestion and modification, we have achieved +10dB at ADC input with this snubber circuit than 22pF, which also prevents ADC malfunction.

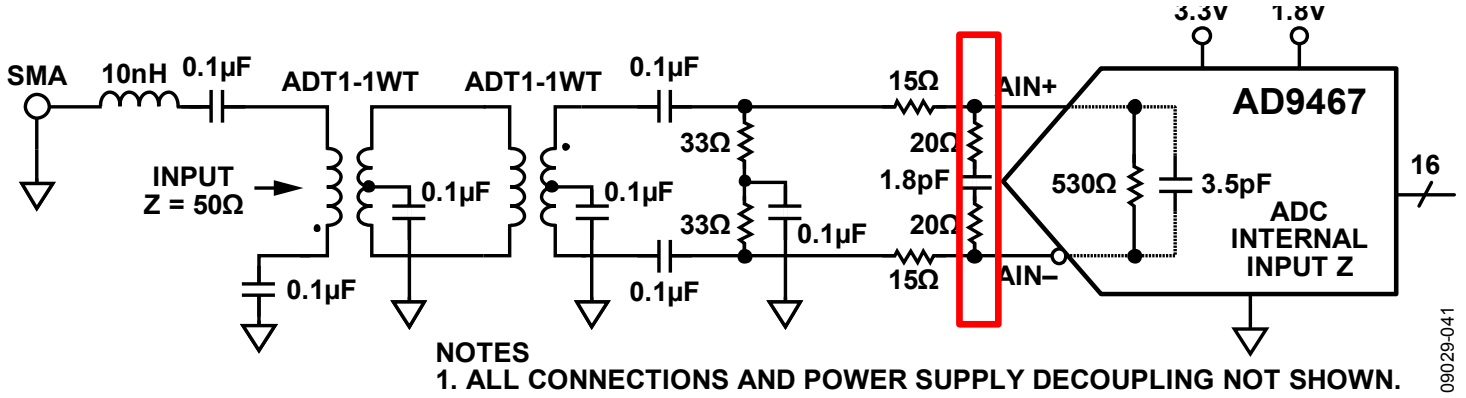
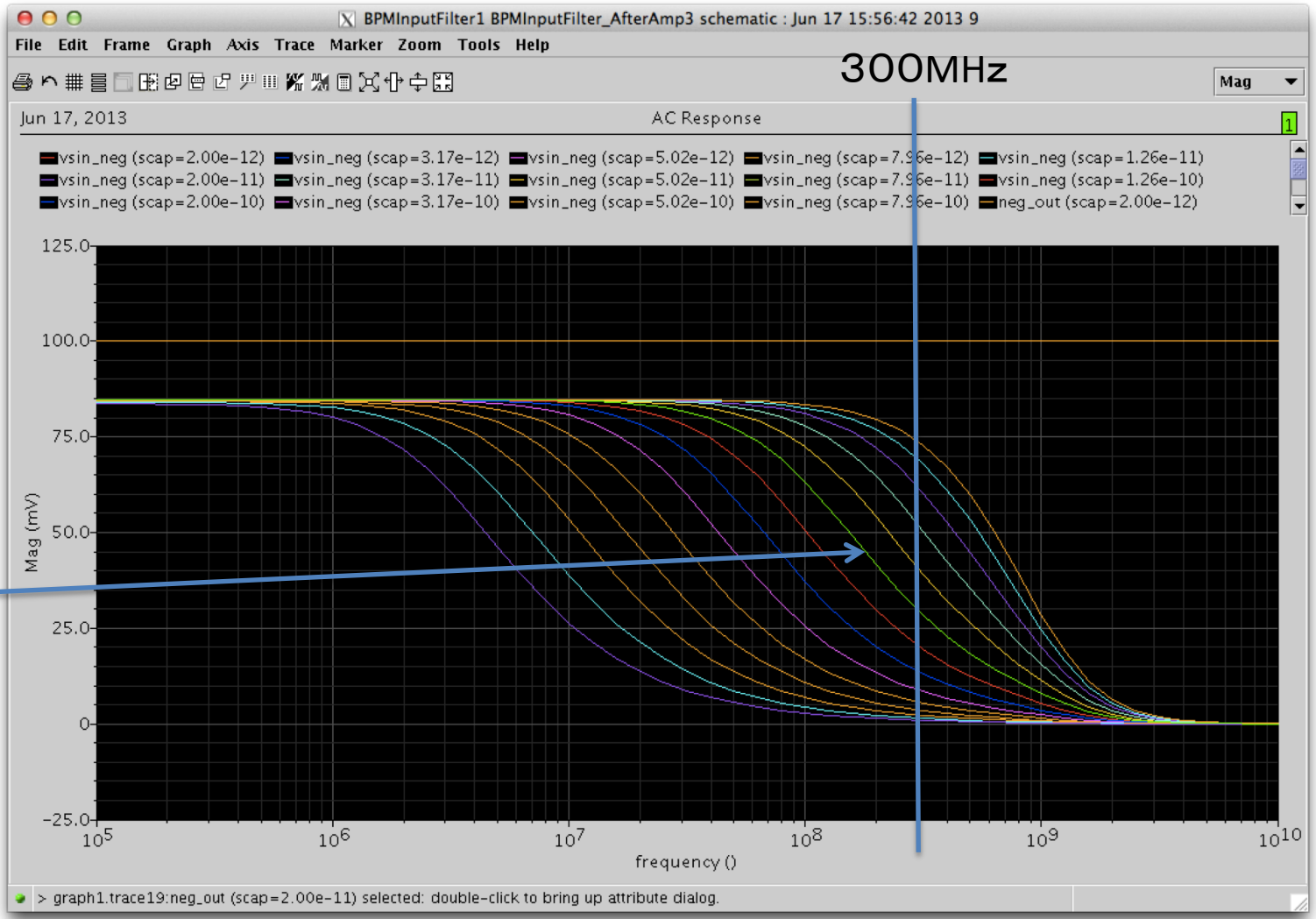


Figure 52. Differential Transformer-Coupled Configuration for IF Applications from 150 MHz to 300 MHz

From ADC9467 Datasheet

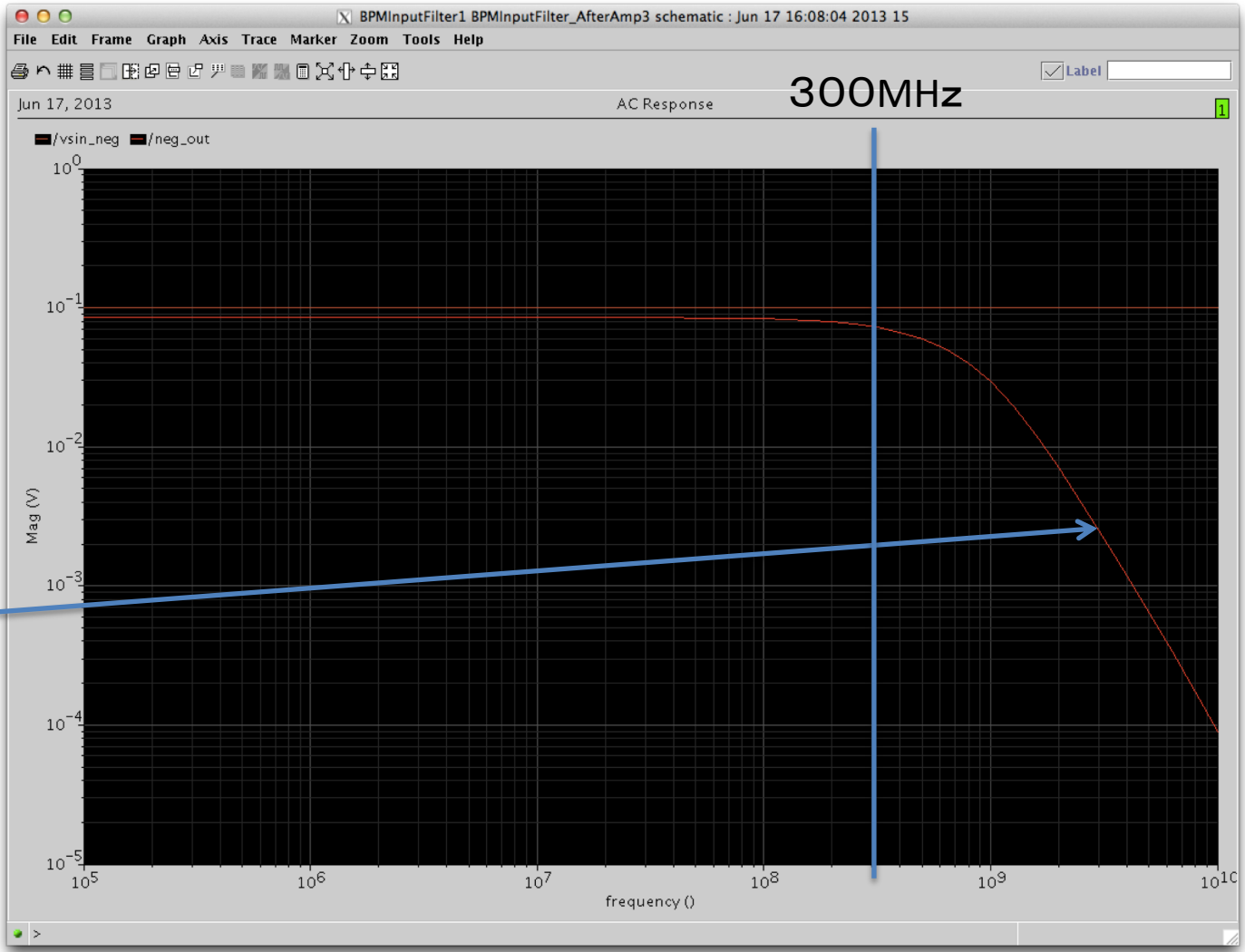
22pF (before modification)

- HSPICE simulation
  - Gain: 1/3 (-10dB) at 300MHz.
  - Lower capacitance behaves unstable, so cannot reduce its capacitance.



Snubber circuit (after modification)

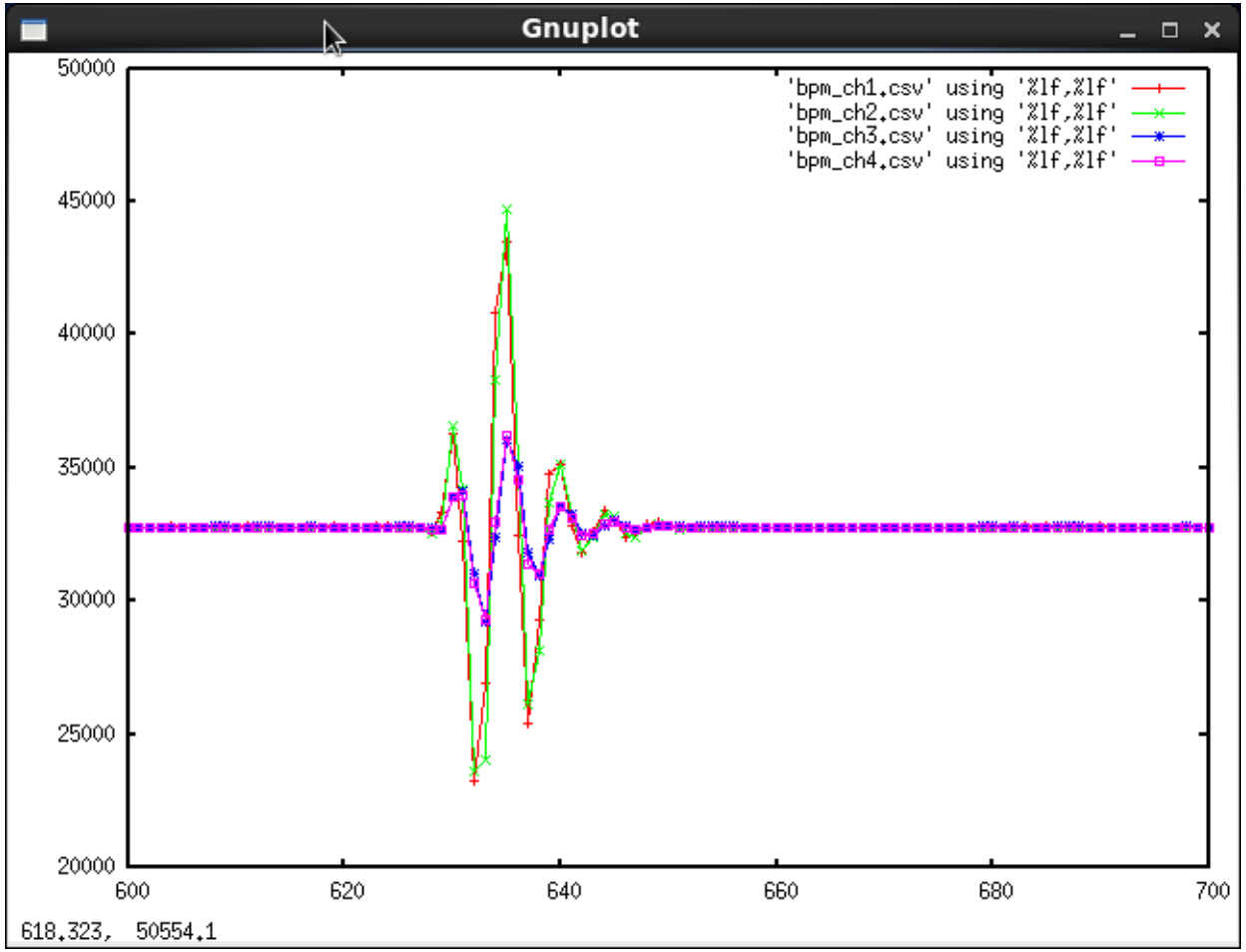
- HSPICE simulation
  - Almost no gain drop at 300MHz.
  - Implement on ch1, ch2 on #2 board.



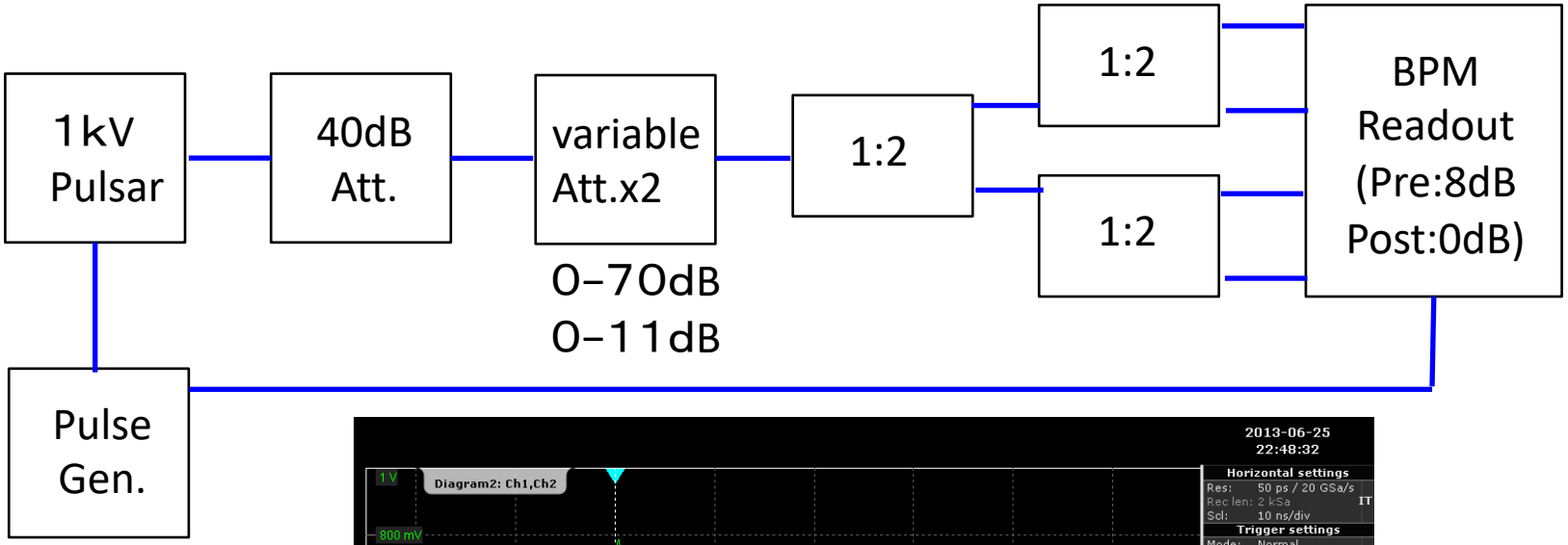
Snubber Circuit

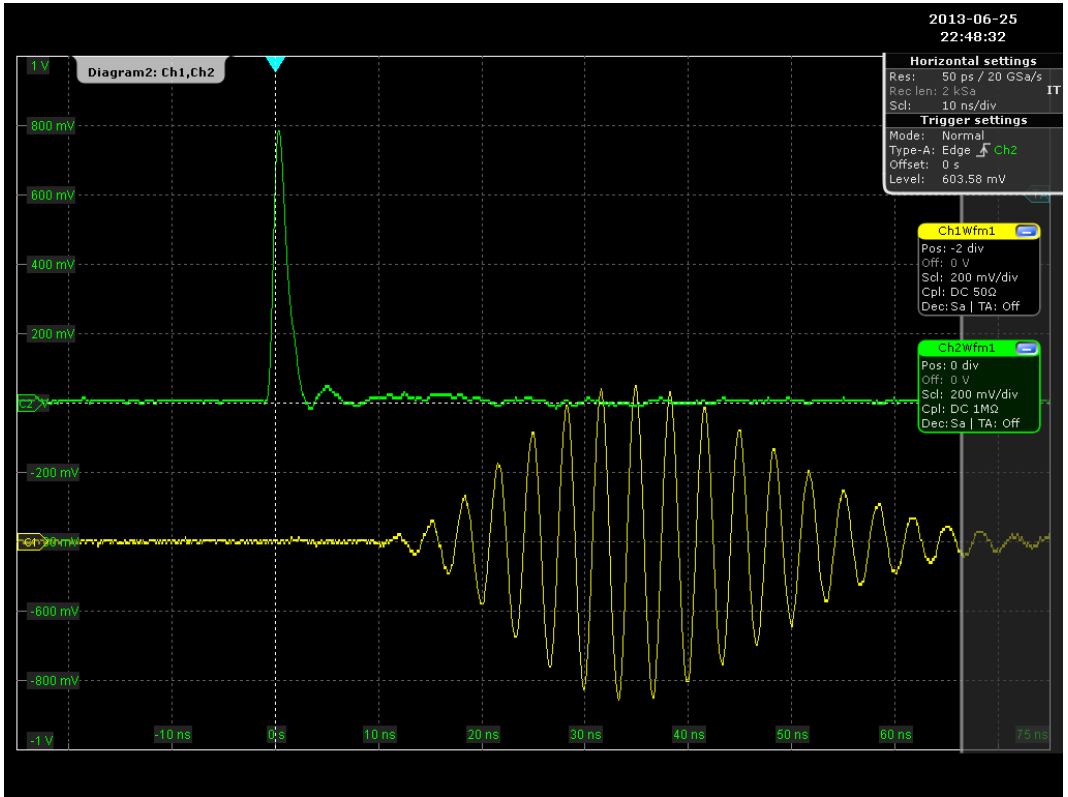
ADC output

- Consistent with calculation. x3 gain (+10dB).
- Proved it also suppress the ADC malfunction.



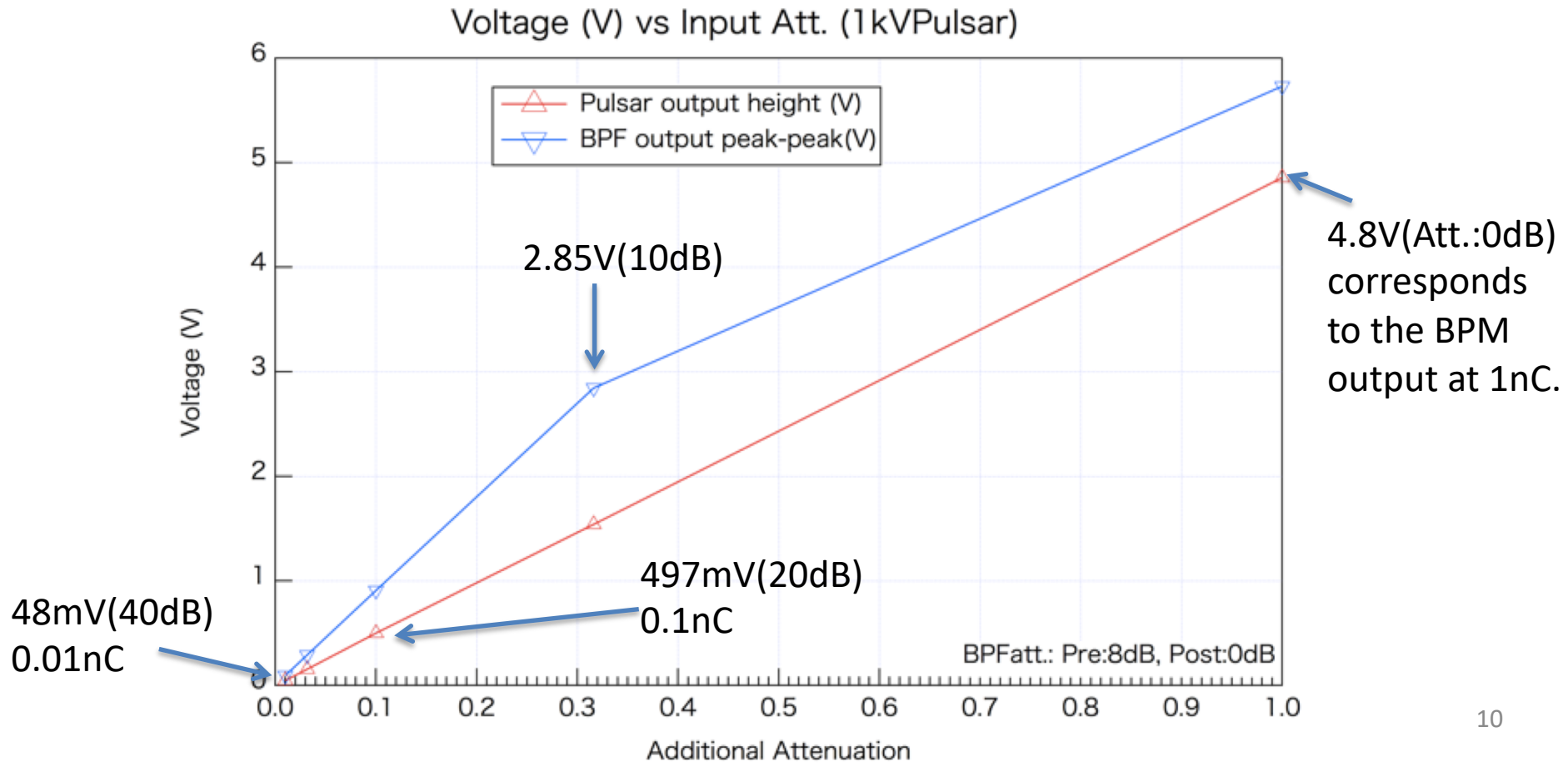
Block diagram of 1kV pulsar test



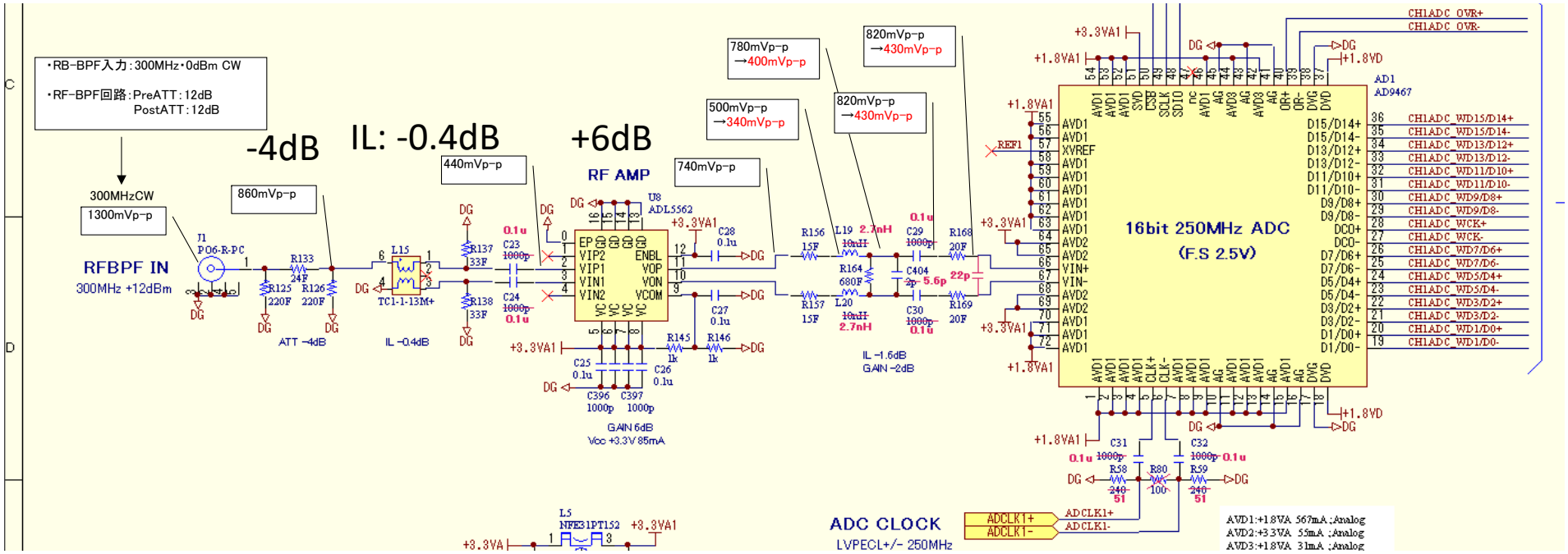


Linearity check (1)

- Attenuator output shows good linearity from 40dB to 0dB.
- BPF output shows good linearity up to 2.85V(10dB) [Spec.2.5Vpp], but after that it shows non-linear behavior. Also lower part of waveform has distortion.



ADC input circuitry

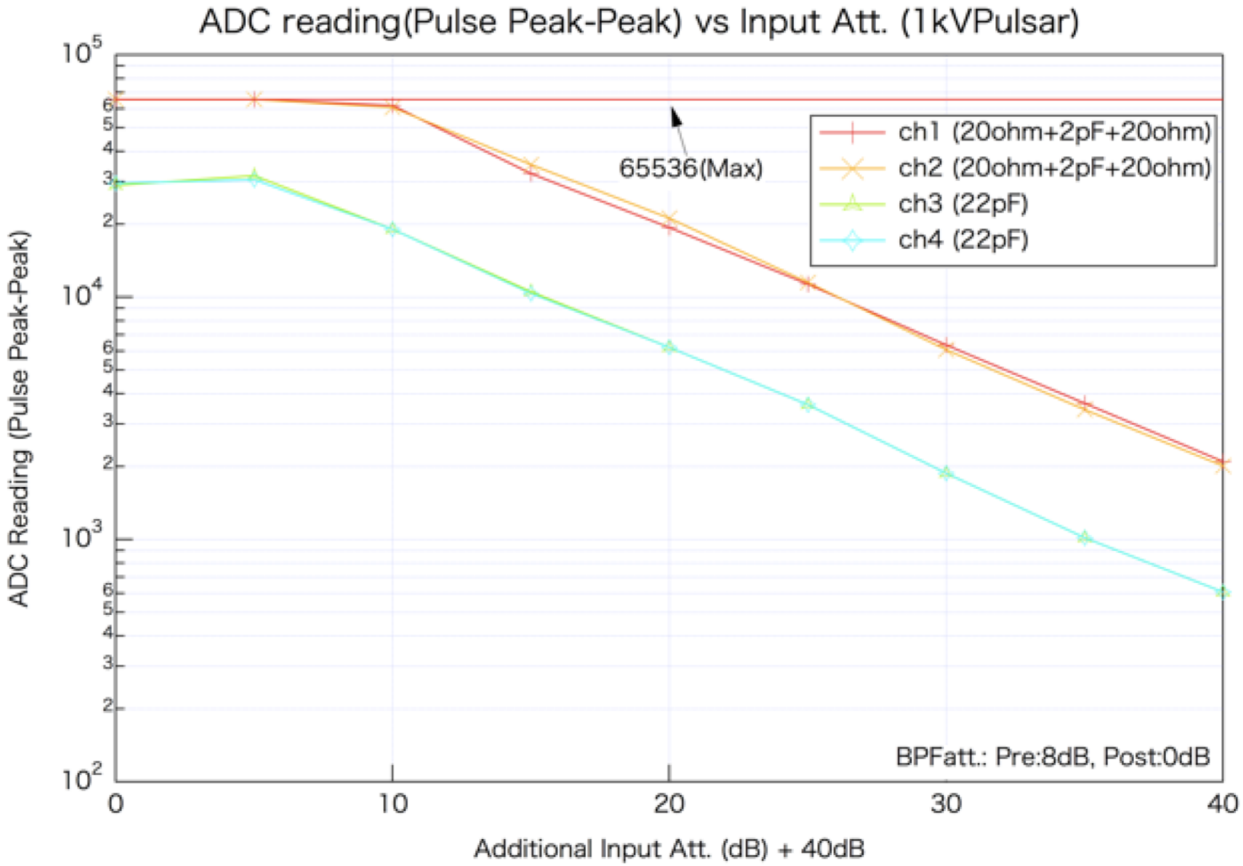


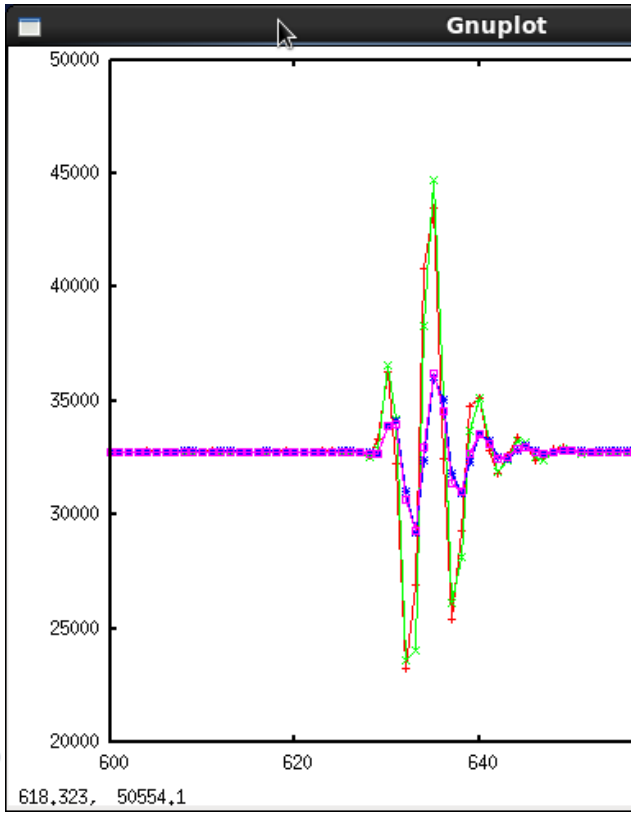
ADL5562
Po1dB=4.9Vpp
(1dB compression point)
-> corresponding input level is 2.46Vpp (11.8dBm).

Acceptable input power:
11.8dBm+4dB+0.4dB=16.2dBm (4.08Vpp)

Linearity check (2)

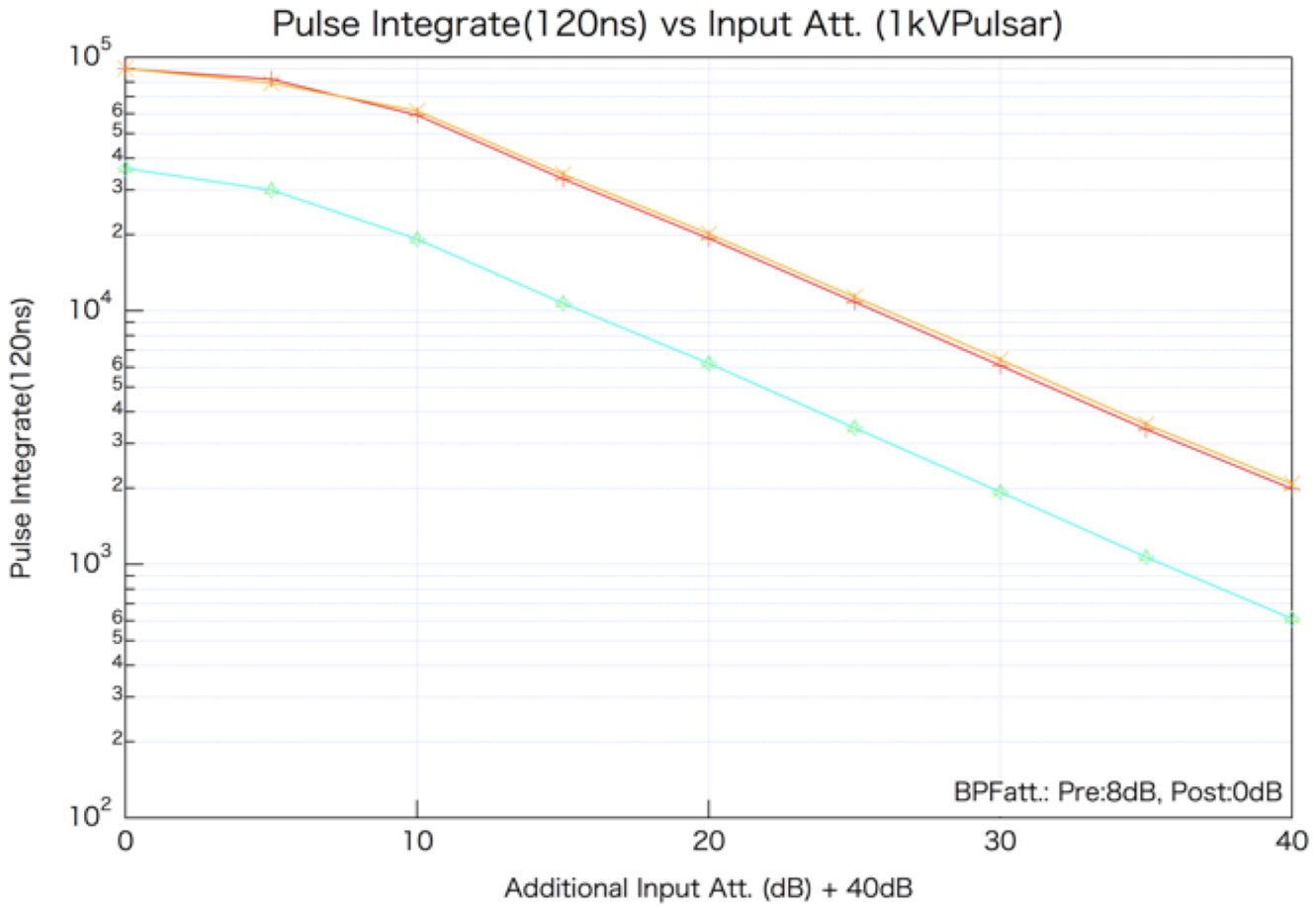
- Semi-Log plot of ADC output peak-peak difference v.s. Attenuator setting.
- ch1, ch2 has x3 (+10dB) gain with snubber circuit.
  - Observed ADC over level at 10dB setting for ch1, ch2 at lower limit (ADC reading is 0).
  - At 0-5dB, ch3 and ch4 have been saturated.
  - In this setting, >10dB attenuator setting is required to keep linearity.





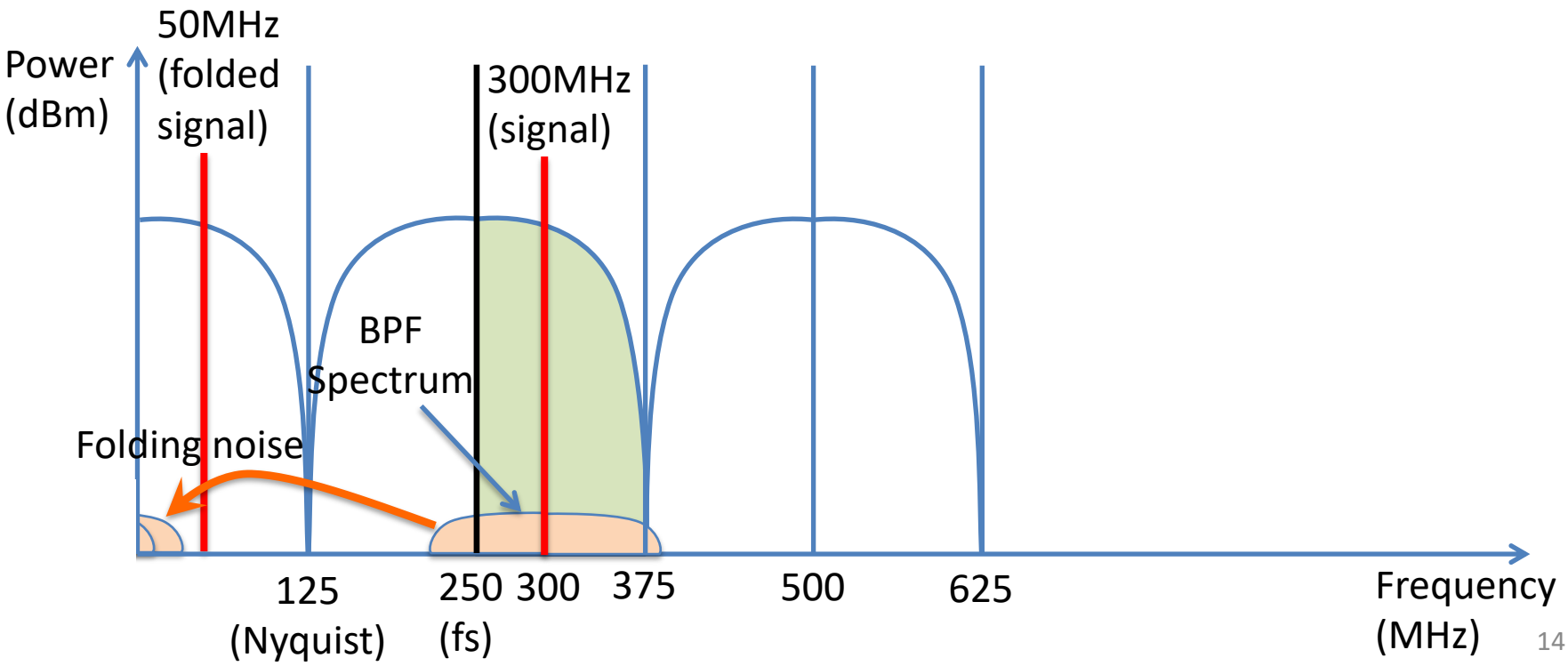
Linearity check (2)

- To check it more precisely, integration of ADC reading (same manner to calculate position resolution) v.s. attenuator setting is shown.
- Also at lower than 10dB, it seems saturation.

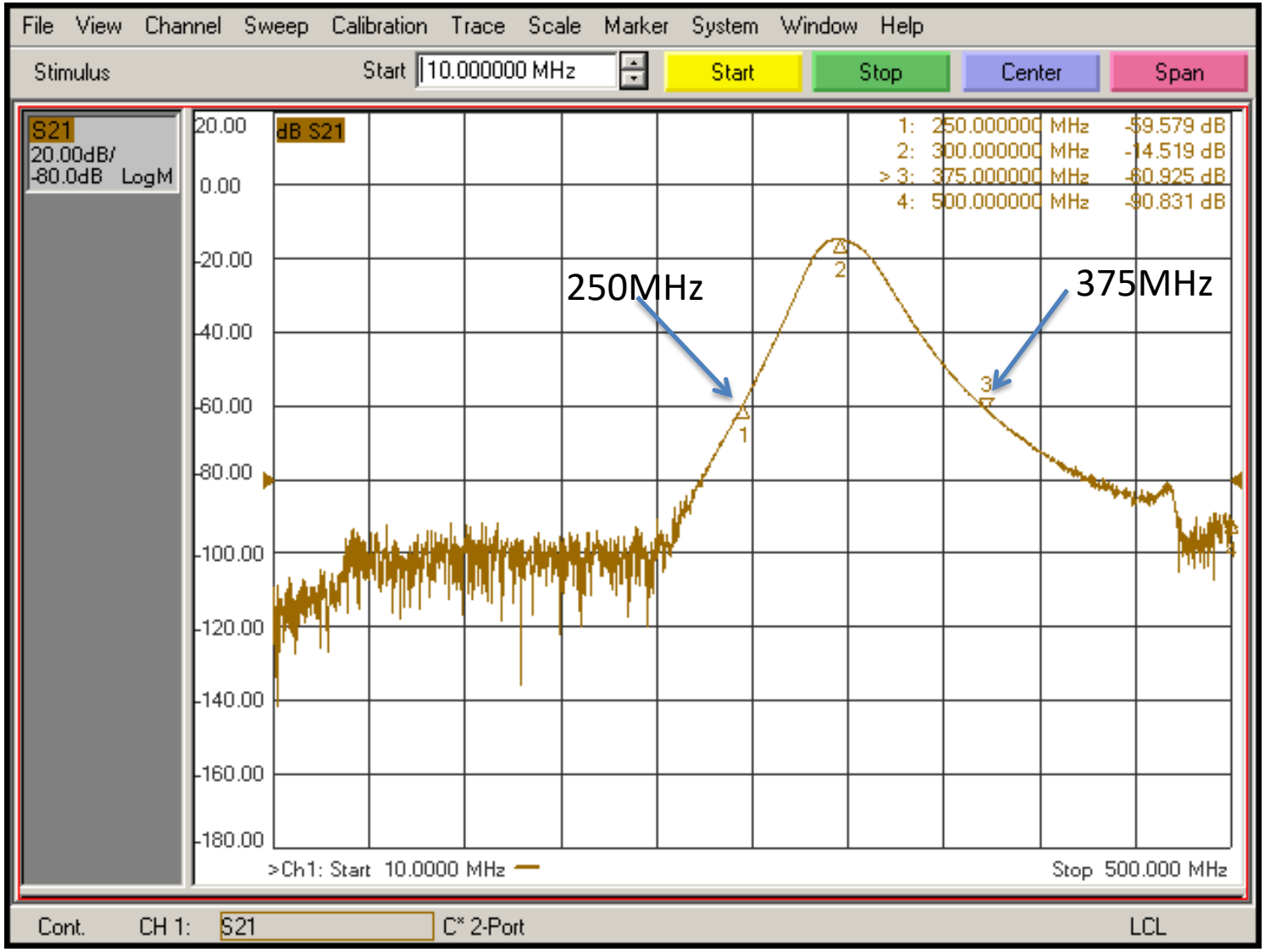


Folding noise at ADC

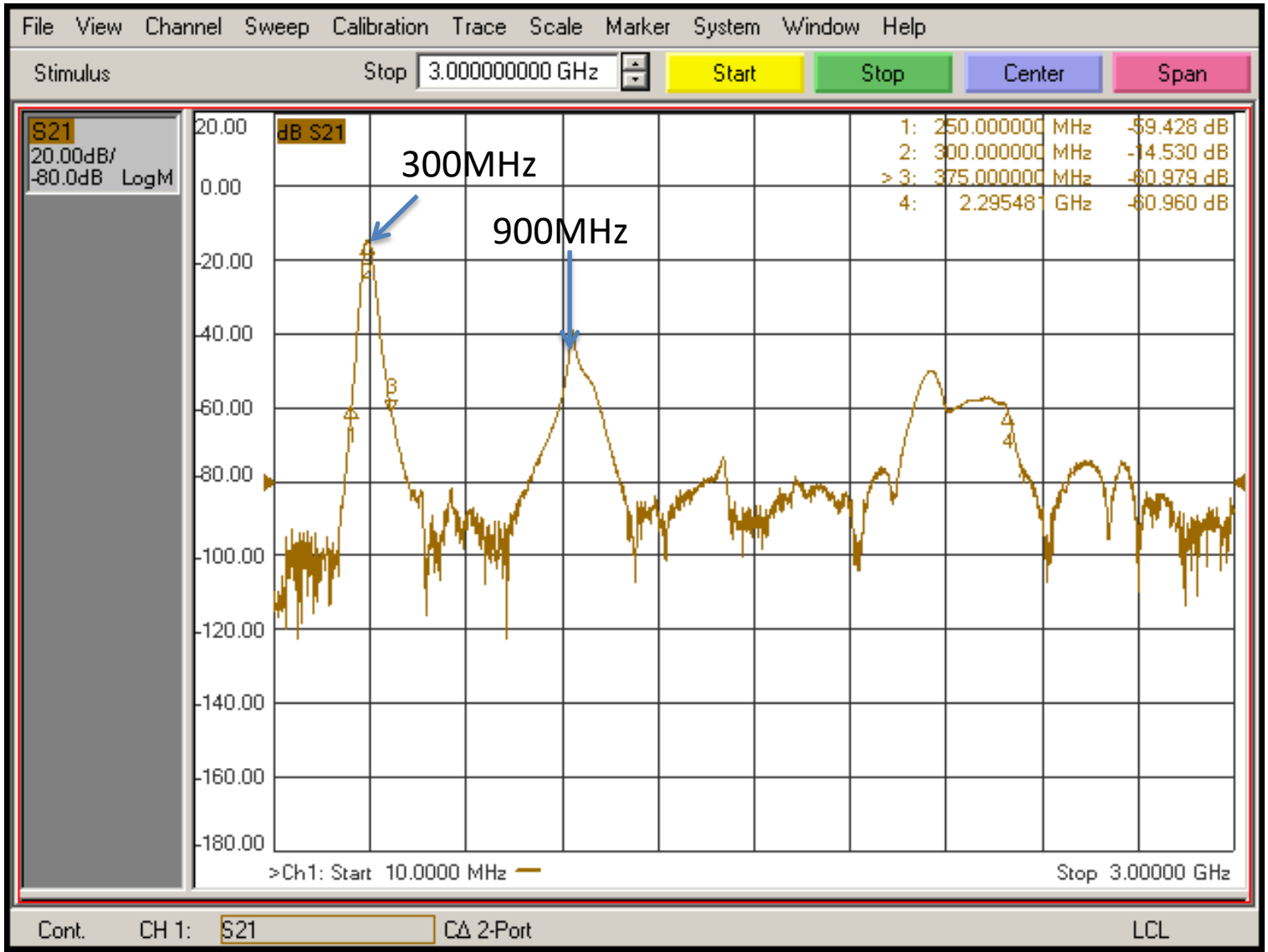
- Tails over the Nyquist window (250MHz - 375MHz) become folding noise.



Frequency response of the Band Pass Filter (S21)

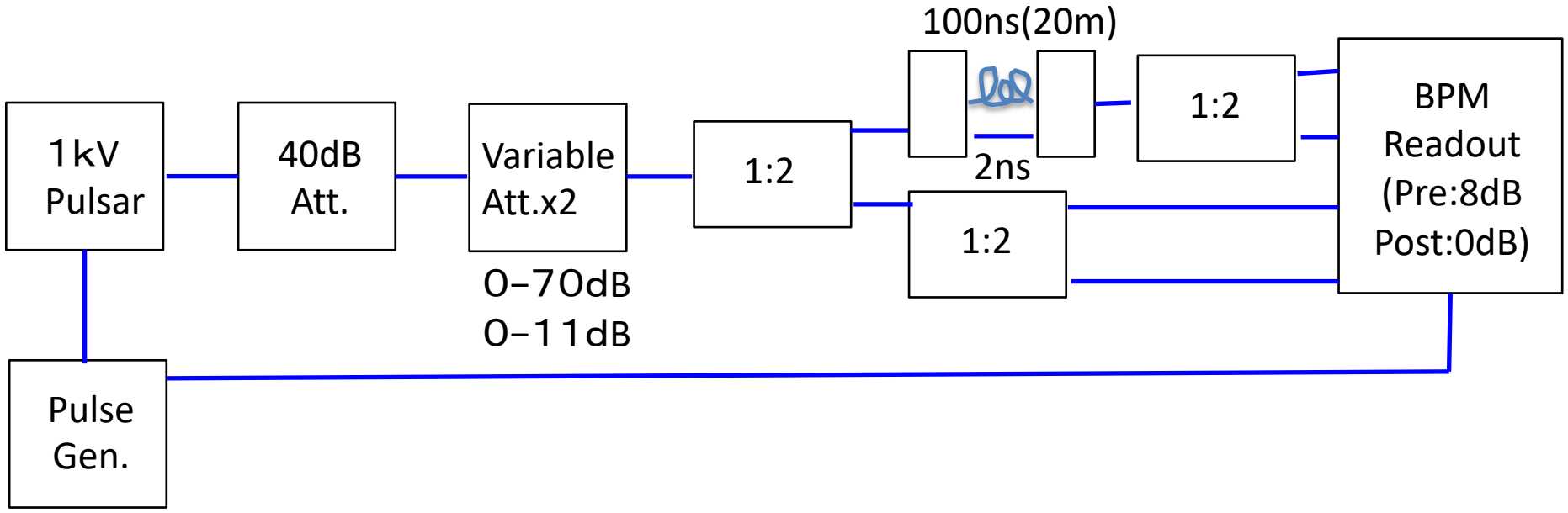


Frequency response of the Band Pass Filter (S21)



Double Pulse test

- To test in more realistic conditions, two bunch signal is emulated by combining 100ns (20m) delayed and 2ns delayed signal. 50 events has been taken with this setting.
  - Att. Pre:8dB, Post:0dB, 40dB+ Additional: 20dB
  - Data: ~ryo/vxworks/work/data/2013June19_exPulsar1kV_no2_doubled/



	1st	2nd
ch1, 2(X)	12.2um	13.6um
ch3, 4(Y)	9.5um	

Harmonics (600, 900MHz) reduction with external LPF

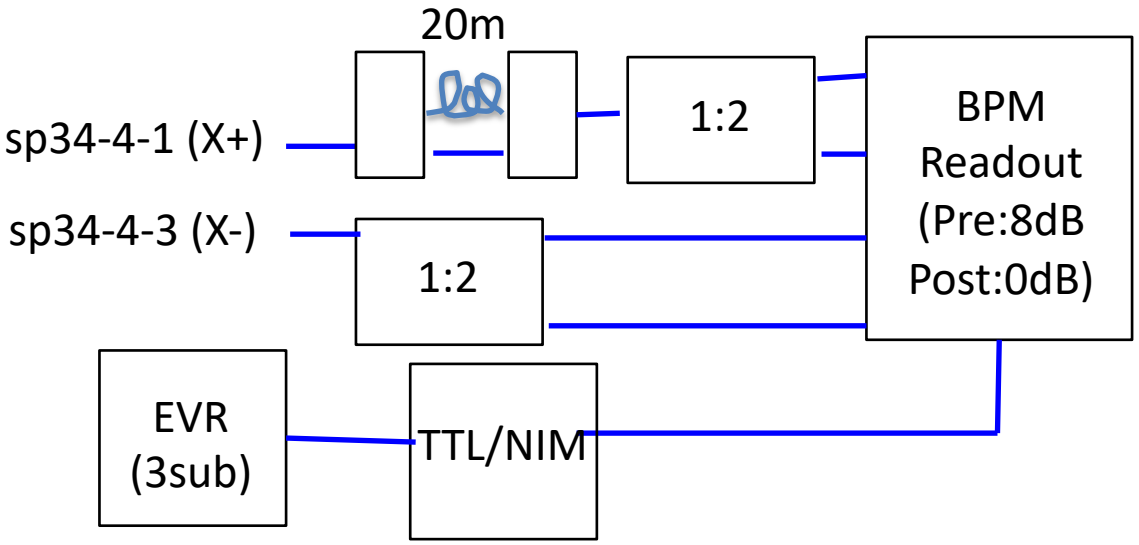
- When 300MHz CW input, double harmonic (600MHz), triple harmonic (900MHz) were observed at about -15dB down to the fundamental.
- When LPF (Mini Circuit VLFX-300) is inserted at BPF output, harmonics have been suppressed to almost the BG level (>53dB suppression). In this setting 100 events data were taken.
  - Att. Pre:8dB, Post:0dB, 40dB+ Additional: 20dB
  - Data: ~ryo/vxworks/work/data/2013June20_exPulsar1kV_no1/

	1st	2nd
ch1, 2(X)	11.9um	14.4um
ch3, 4(Y)	9.8um	

- No significant difference were observed.

Beam Test

- As we can get about 10um position resolution constantly with pulsar, we confirmed it with beam signal.
- Beam signal were divided to two input signal to emulate ideal (no beam position jitter) beam signal.



Beam Test (cont'd)

- 300events data were taken.
  - @3-2, PFE 5Hz, 0.3nC
  - Att. Pre:8dB, Post:0dB <= Set this value to keep input <3Vpp.
  - Data: ~ryo/vxworks/work/data/2013June19_beam_ch12fanout_doubled_ch34_fanout/

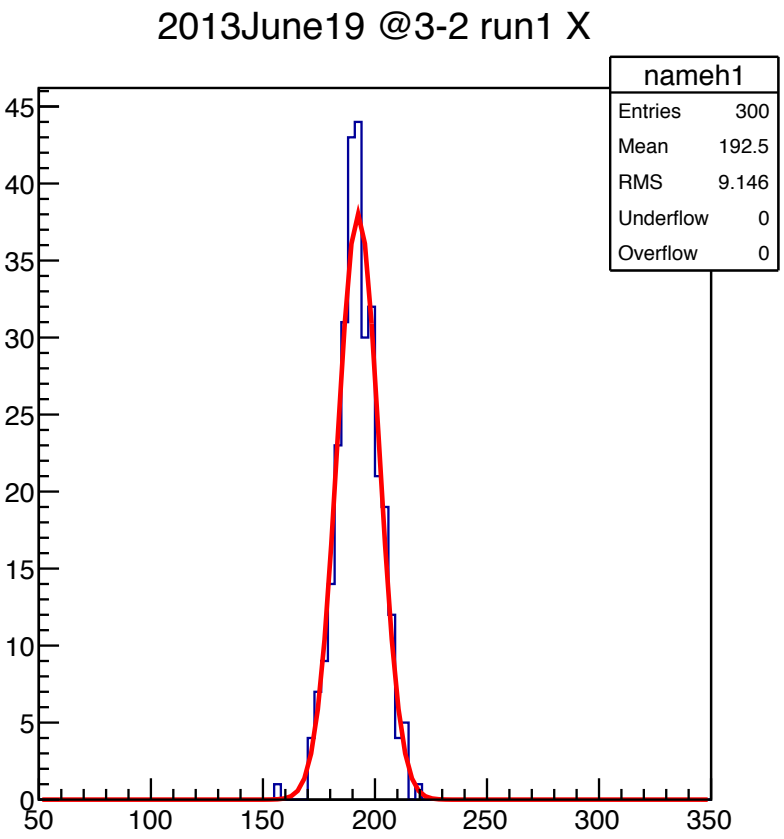
	1st	2nd
ch1, 2(X)	11.9um	14.4um
ch3, 4(Y)	9.8um	

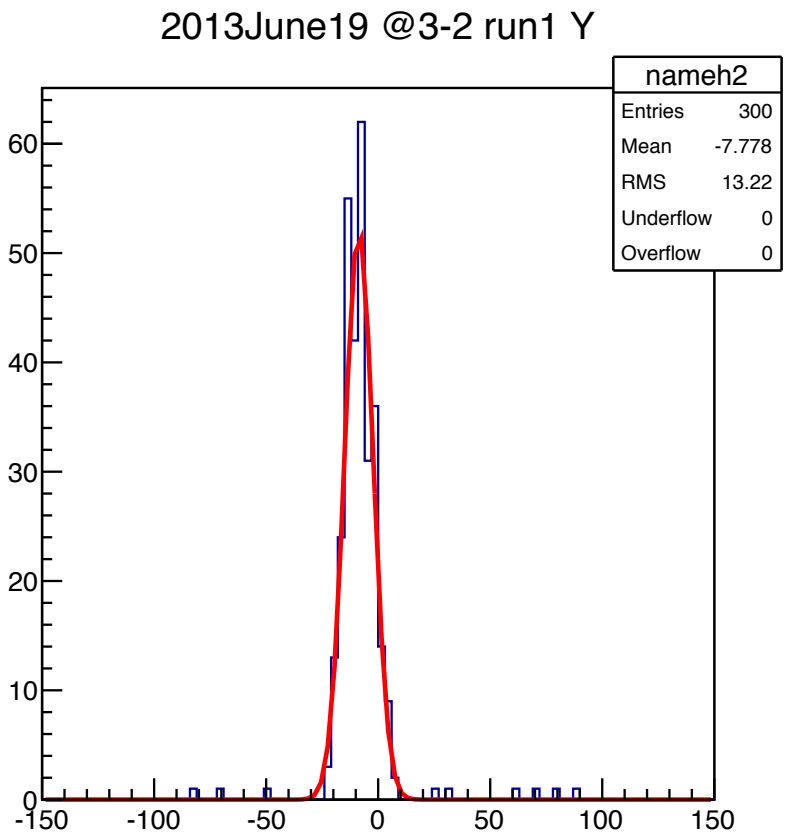
- At previous test (May 29th):
  - @3-2, PFE 1Hz, 0.5nC
  - Att. Pre:0dB, Post:0dB single pulse
  - Data: ~ryo/vxworks/work/data/2013May29_beam_ch12fanout_ch34fanout/

ch1, 2(X)	53.8um
ch3, 4(Y)	30.7um

- Confirmed that the worse position resolution were caused by input saturation.

Beam test (cont'd)





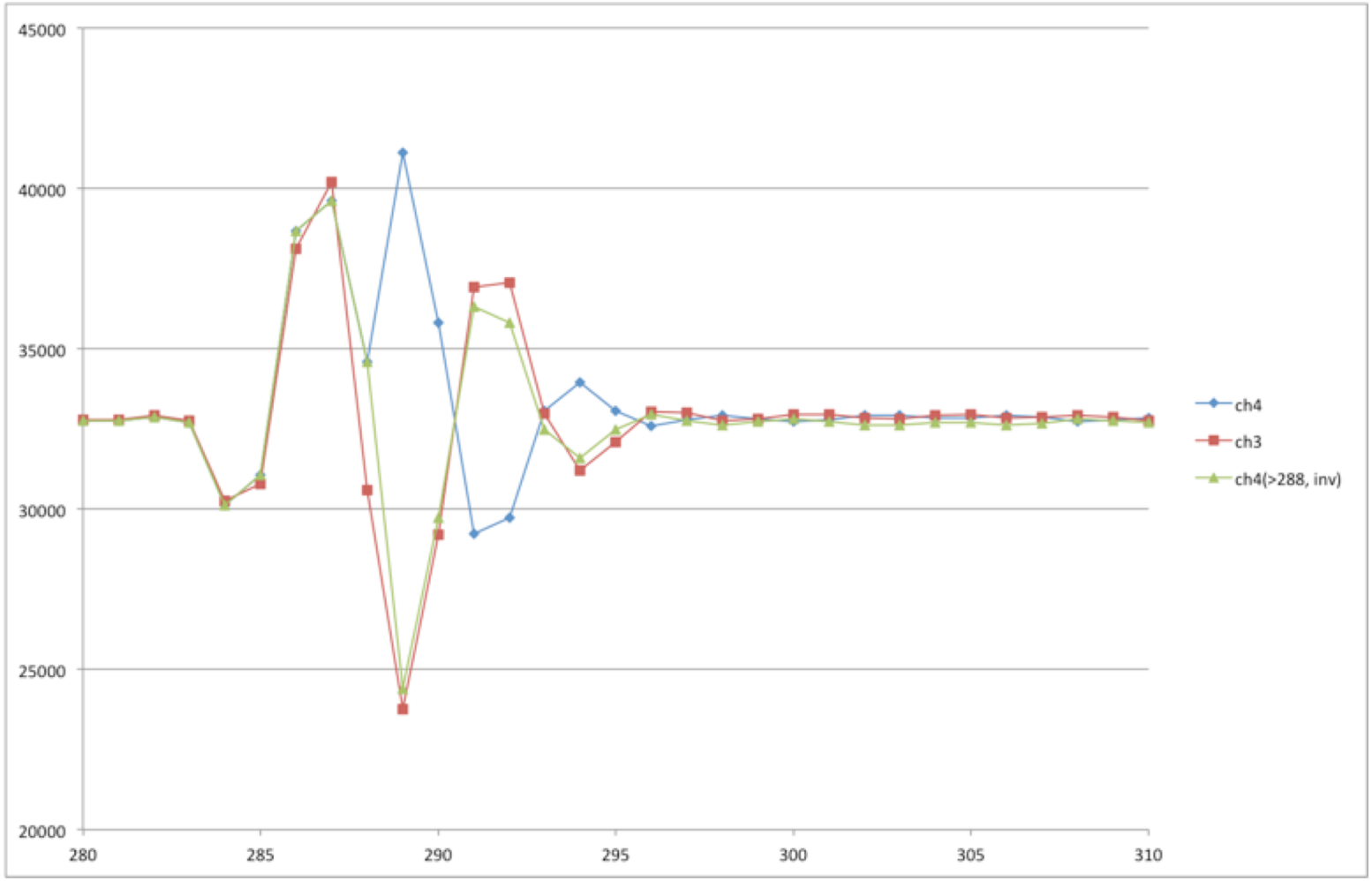
Beam Test (cont'd)

- 100 events were taken with 0.45nC.
  - Att. Pre:8dB, Post:0dB, 40dB+ Additional: 20dB
  - Data: ~ryo/vxworks/work/data/2013June19_beam_ch12fanout_doubled_ch34_fanout-no2/
  - Event#59 were rejected from analysis because it contains ADC malfunction.

	1st	2nd
ch1, 2(X)	5.7um	8.2um
ch3, 4(Y)	5.1um	

- Better position resolution than 0.3nC. Position resolution may be limited by signal source S/N. (i.e. 1kV pulsar might have not a good S/N than high charge beam.)

#59 event data



- Suddenly waveform sign were inverted after time > 288
  - Have to check ADC clock delay IC.