THE DATA ACQUISITION SYSTEM BASED ON SoC FPGA FOR THE MAGNET POWER SUPPLIES IN J-PARC MR

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Abstract

The current ripple is significant to the beam quality. All these elements are closely related to the data acquisition probe, Analog-to-Digital Converter (ADC). In this paper, a data acquisition system based on System-on-Chip (SoC) Field Programmable Gate Array (FPGA) for ADC data readout is described. Moreover, the results of a typical ADC, multi-channel, Successive Approximation Register (SAR) ADC AD7616 are measured and discussed.

INTRODUCTION

A series of upgrades about the power supplies for the bending, quadrupole, and sextupole magnets have been conducted to increase the beam power in the Japan Proton Accelerator Research Complex (J-PARC) Main Ring (MR) [1 - 2]. The beam power has reached 800 kW which is an important milestone in 2024. To the final goal of 1.3 MW, the current ripple of the magnet power supply is very important because the current has a direct relationship with the magnet field and the beam tuning.

Usually, we use current deviation which is defined by [3]

$$\frac{\Delta I}{I} = \frac{I_{sample} - I_{ref}}{I_{ref}} \quad (1)$$

to describe the current ripple. Here I_{sample} is the current measurement result of the Analog-to-Digital Converter (ADC), I_{ref} is the reference current of the power supply output. The ADC is an essential sensor to obtain current ripple in a magnet power supply, and the reason is listed as follows:

Firstly, in the power supply current feedback control loop, the performance limitation of the current ripple is determined by the current sensor including ADC and DC Current Transformer (DCCT). For example, it is difficult to obtain a higher resolution current than the ADC resolution bit or a higher frequency current component than the ADC sampling frequency.

Secondly, it is necessary to monitor the power supply output current and give an effective current correction or compensation system for beam improvement. For example, A real-time correction of the betatron tune ripples is designed based on the measurement and prediction of the bending and quadrupole magnet power supplies, which improves the spill quality in slow extraction [4]. A real-time COD correction system for the high-intensity proton synchrotrons is used by obtaining the current ripple of the bending magnet and adding a compensation current pattern to the steering magnet [5]. For the measurement function, the ADC is required.

Thirdly, although it is not so complex to make the ADC work, usually including the peripheral circuit design and driver development, how to read the ADC data out and then analyse the data during the first development phase is also indispensable. For example, it is helpful that the ADC data is saved in a file using storage memory and the data can be analysed anytime. This is usually the first step of the real-time correction system development.

In this paper, a data acquisition system based on System-on-Chip (SoC) Field Programmable Gate Array (FPGA) for the magnet power supplies in J-PARC MR is proposed. This system is mainly focusing on providing a platform for ADC development. A multi-channel Successive-approximation (SAR) ADC, AD7616 is used, and its measurement results are presented and analysed.

SCHEMES

The purpose of the data acquisition system is to provide a platform for evaluating different ADCs which can be the candidates for magnet power supplies. To achieve this purpose, two important basic functions should be considered. The first one is the ADC driver development. The second one is the data file process system which can store and analyse the ADC data. For the ADC driver, since there are many kinds of driver interfaces such as Serial Peripheral Interface (SPI) and parallel interfaces, the main processor should be convenient to provide different kinds of such interfaces. The Field Programmable Gate Array (FPGA) is a good choice since it has advantages in parallel computation functions which can make full use of high-speed ADC usage and user can design their interface timing freely based on the ADC design requirement. For the data file processing, Advanced RISC Machine (ARM) is a good option. It can provide a Linux operating system platform that supports thoroughly the file system.

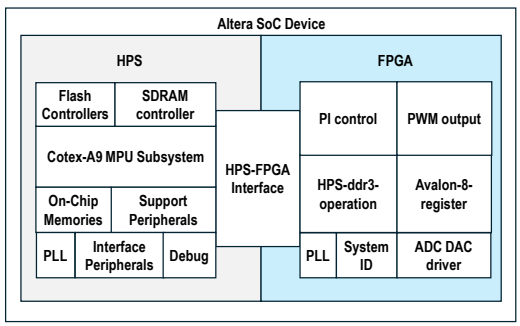

Figure 1: Altera SoC FPGA.

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Based on the above analysis, how to combine both the FPGA and ARM usage and make full use of them becomes an important topic. As shown in Fig. 1, the SoC chip provided by Intel Altera is chosen, consisting of the FPGA and ARM (also called Hard Processor System, HPS) with developed communication bridges [6].

SYSTEM DESIGN

The hardware and software design of the data acquisition system is presented in this part.

Hardware

Figure 2 shows the data acquisition system hardware layout. The system consists of three parts, the input, processor, and memory unit. The input unit is mainly the ADC board which will be described in detail later. The processor unit is CYCLONE V FPGA 5CSEBA6U2317. The memories include 1GB DDR3 SDRAM and 4GB SD Card. Table 1 lists the chips and evaluation board selection. The input part which includes ADC and interface can be replaced by other ADC for different usage.

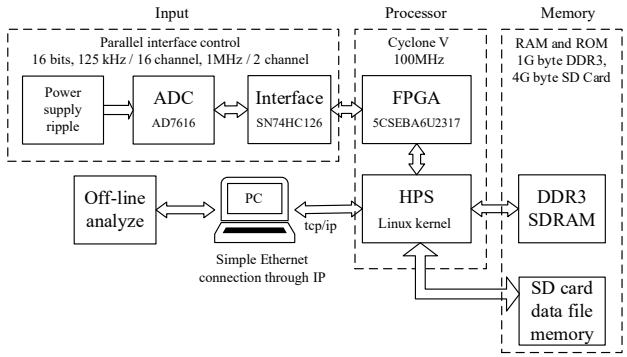

Figure 2: Layout of the data acquisition system hardware.

Table 1: Evaluation Boards Selection

Item	Chips	Evaluation Board
FPGA	5CSEBA6U2317	DE10-NANO
ADC	AD7616	EVAL-AD7616SDZ
Interface	SN74HC126	Self-designed board

Software

Table 2: Key Modules in SOPC System

Item	Description	Type
SDRAM_WR_RD	Ping-pong operation of HPS SDRAM memory	Customized IP core
Register	8 bits data width Avalon Memory Mapped Slave	Customized IP core
HPS	Cyclone V Hard Processor System	Altera IP core
PLL	Altera PLL	Altera IP core

The software includes 2 parts, the firmware part which is implemented in FPGA, and the software part, which is accomplished in HPS. Based on the interface provided by Altera, some flag and control signals can be exchanged between FPGA and HPS.

The key modules of the System-On-a-Programmable-Chip (SOPC) system and their function descriptions are listed in Table 2. Except for that, the ADC driver and power-on-reset module are designed in the FPGA part but not embedded in the SOPC System.

FPGA To avoid the conflicts between writing and reading in HPS Synchronous Dynamic Random-Access Memory (SDRAM), the ping-pong reading and writing operation shown in Fig. 2 is designed which means that 2 memory parts being written and read are designed. For example, if RDOUT A is being written but not finished writing the total preset data length, the data in RDOUT A is locked and cannot be read. Only if one whole waveform which reach the preset data length is written, this waveform data can be read. In this way, the read-out data can be kept continuous and complete.

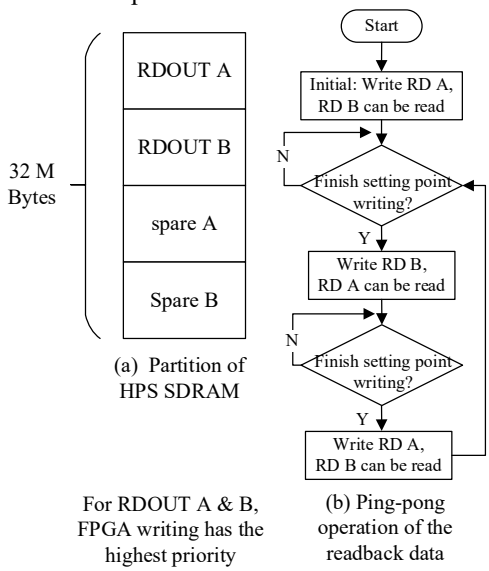

Figure 3: SDRAM partition and logic.

HPS A 1 G Bytes DDR3 SDARM is distributed in the HPS part which can be used as the Linux system cache in the DE10-NANO board. Based on the FPGA to HPS slave bridge, this cache SDRAM can also be accessed by FPGA. Because of the Linux kernel memory management mechanism, to avoid the writing and reading conflict, a continuous part of memory has to be applied by using the kernel malloc function and install the kernel malloc module before memory usage by FPGA.

After the memory application, the ADC data is written to the RDOUT A or RDOUT B area by FPGA. An application about writing and reading data has been designed in HPS, so the user can choose manual mode or automatic operation mode for memory operation. After writing, the data can be read out and stored in a data file using an SD card. If necessary, online and offline data analysis can be conducted. For example, Fast Fourier transform (FFT) can be done by FPGA part and result data can be stored by the same method.

ADC EXPERIMENT

There are different kinds of ADCs, including Flash ADC, pipeline ADC, SAR ADC, charge balance ADC and sigma-delta ADC. Reference [7] gives some suggestions about how to choose the ADC based on the ADC type characteristics. Table 3 shows the comparison of SAR ADC and sigma-delta ADC. Because the bandwidth, resolution, and latency are concerned, a 16-channel and 16-bit SAR ADC, AD7616 is chosen for the data acquisition system.

Table 3: ADC Performance Comparison

ADC	SAR	Sigma-delta
Throughput	Good	Fair
Bandwidth	Very good	Fair
Resolution	Very good	Excellent
Latency/Hz	Very good	Fair
Linearity/bit	Fair	Very
Multiplexing	Very good	Poor

To observe the ADC output data directly, during the experiment, an evaluation board of 16-bit DAC AD5764 with 4 channels driven by the FPGA is used. There are two functions of this DAC. One is for a signal source for the ADC input and the second is for monitoring by converting the digital data to an analog signal. This function can be selected through register module.

To achieve multi-channel and high-rate throughput usage, the parallel working mode is used for the AD7616. After a global reset, the procedure of writing the configuration of the first channel and obtaining CH0A and CH0B data are conducted. And then the same procedure is repeated for the next seven channels. Finally, the data of a total of 16 channels can be obtained. For each conversation, CHA and CHB are sampled and finished at the same time, which means that the synchronous data can be read out. All these procedures are finished in a finite-state machine (FSM). The bidirectional 16-bit signals work in a Time Division Multiplexing (TDM) way. Namely, they act as the configuration signal and data signal in different period.

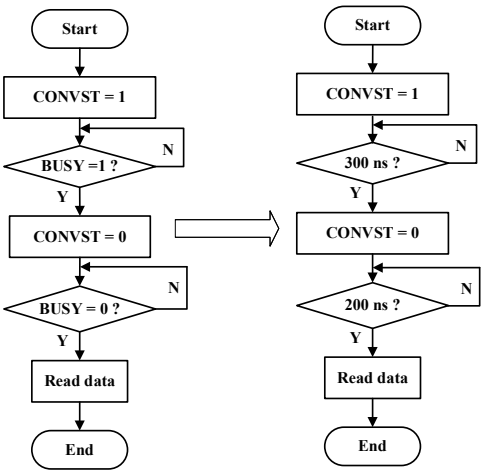

Figure 4: AD7616 free running mode.

However, during the testing phase, we find that the BUSY and bidirectional 16-bit signals are susceptible to the noise. As shown in the left block diagram of Fig. 4, because the original FSM works based on the BUSY, the FSM will stop because of the glitch of BUSY. To avoid this error, the AD7616 is designed to work in a free-running mode which is shown in the right block diagram of Fig. 4, i.e. a timing of keeping a constant value of CONVST but ignoring the BUSY is used.

To overcome the instability of the bidirectional signal, an interface circuit with isolation is designed using SN74HC126, as shown in Fig. 5. The SN74HC126s act as a buffer with 3-state function and noise suppression.

After using the free-running mode and the interface board, the ADC output becomes stable.

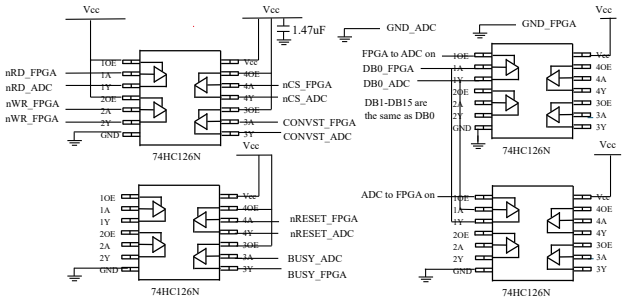

Figure 5: Schematic of the interface board.

RESULT AND ANALYSE

AFG Output Measurement

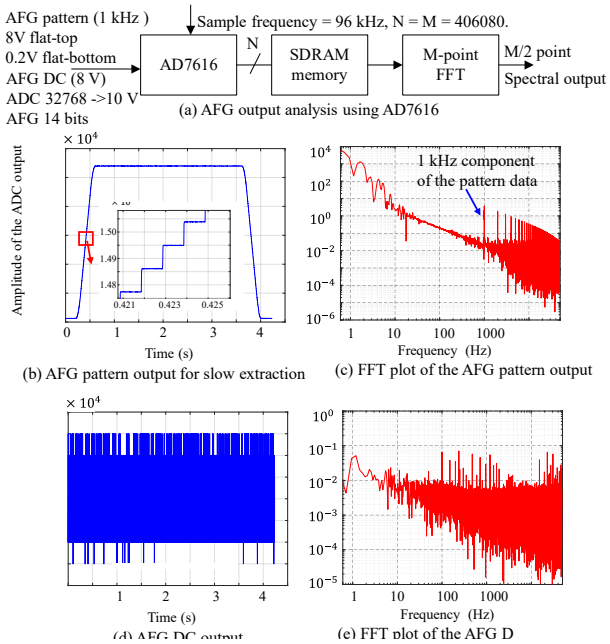

Figure 6: AFG output measurement and analysis.

A Tektronix Arbitrary/ Function Generator (AFG) 3022B is used as the signal source to test the system. As

shown in Fig. 6 (a), a current pattern waveform output of the trim coil for sextupole magnet and a DC output of the flat-top value are measured. The pattern data is generated in the control network, sent, and stored in the AFG. The frequency of data is 1 kHz. Using the data acquisition system, ADC output data is written in the HPS DDR3 SDRAM, and the corresponding data is read by HPS. A data file is generated by HPS and is sent to the host computer. FFT analysis is conducted by the host computer. Figure 6 (b), (d), and (c), (e) are respectively the time domain plot and the FFT spectrum diagram. Because the original data frequency is 1 kHz, the output of the AFG has a series of 1 kHz component in the FFT plot.

DAC AD5764 Output Measurement

Using the pattern of bending magnet power supply from the J-PARC Control network, a pattern is converted to an analog signal by DAC AD5764. The frequency of data is 96 kHz. After replacing the AFG with DAC, the same measurement and analysis as AFG are conducted. The series plots are shown in Fig. 7. Compared to the AFG output, the DAC output has a cleaner harmonic component.

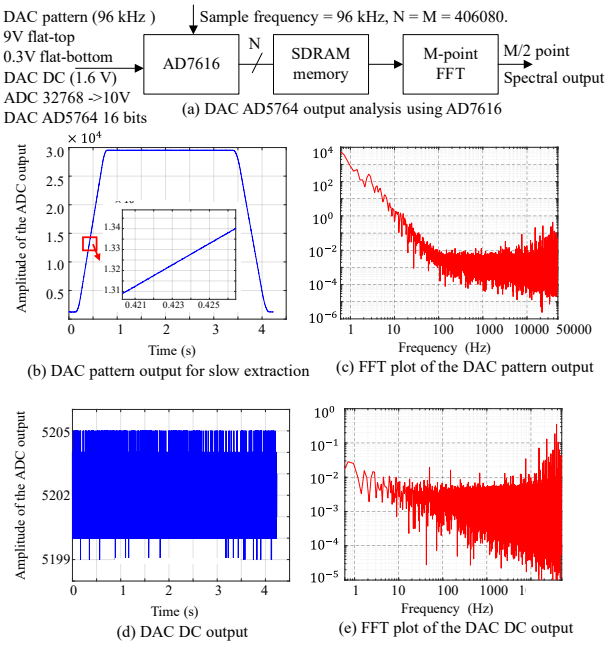

Figure 7: DAC AD5764 output measurement and analysis.

SUMMARY

A data acquisition system based on SoC FPGA is proposed in this paper, which is prepared for the J-PARC Main Ring magnet power supply. To verify the feasibility of the data readout function, a multi-channel SAR ADC AD7616 is used as the sampling component, and a multi-channel DAC AD5764 is used as the signal. The AFG and DAC output are tested using the data acquisition system, which will give a reference for the sextupole trim coil power supply design in J-PARC MR.

REFERENCES

[1] T. Shimogawa *et al.*, "A control system of new magnet power converter for J-PARC main ring upgrade", *IEEE Trans. Nucl. Sci.*, vol. 66, no. 7, pp. 1236-1241, Jul. 2019. doi:10.1109/TNS.2019.2899380

[2] Y. Morita *et al.*, "Upgrading magnet power supply system in J-PARC Main Ring", in *Proc. 14th Int. Particle Accelerator Conf. (IPAC'23)*, Venice, Italy, May 2023, pp. 3762-3765. doi:10.18429/JACoW-IPAC2023-WEPM082

[3] M. Tomizawa *et al.*, "Tracking error analysis on the power supply currents of J-PARC main magnets", in *Proc. 15th Int. Particle Accelerator Conf. (IPAC'24)*, Nashville, U.S., May. 2025, pp. 1665-1668.

[4] D. Naito *et al.*, "Real-time correction of betatron tune ripples on a slowly extracted beam", *Phys. Rev. Accel. Beams,* vol. 22, p. 072802, Jul. 2019.

[5] T. Asami *et al.*, "Development of real-time COD correction system for the high intensity proton synchrotrons", in *Proc. 17th Annual Meeting of Particle Accelerator Society of Japan (PASJ'20)*, Online, Japan, Spe. 2020, pp. 20-24.

[6] *Cyclone V Hard Processor System Technical Reference Manual*, 101 Innovation Drive, San Jose, CA 95134, Aug. 2023, pp. 2-3, https://cdrdv2.intel.com/v1/dl/getContent/666962?fileName=cv_5v4-683126-666962.pdf

[7] J. Pickering, "Analogue to digital and digital to analogue converters (ADCs and DACs): A review update", *arXiv preprint arXiv*, 11607.01589, 2016.