BEAM STABILIZATION AT KEK LUCX FACILITY BY DIGITAL LLRF PHASE&AMPLITUDE FEEDFORWARD IMPLEMENTATION INTO RF SYSTEM

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Abstract

The KEK LUCX facility is a normal conductivity multi-bunch linear electron accelerator. It focuses on developing and operating a high-power monochromatic X-ray source for imaging purposes. The X-ray parameters, such as energy, energy bandwidth, temporal structure, and flux, are determined by the characteristics of the multi-bunch beam and the laser pulses train. From the accelerator side, the absolute values of these X-ray parameters depend on electron beam characteristics like transverse normalized emittance, average energy, energy spread (RMS), bunch charge, bunch length, and its arrival time. Furthermore, all these characteristics depend on the the accelerating field absolute values of the phase and amplitude. The Low Level Radio Frequency (LLRF) system controls the phase and amplitude, making the choice of LLRF signal distribution architecture a crucial initial step in developing the LLRF system. This paper outlines the new LLRF system architecture at the KEK LUCX facility and discusses the Laser-to-RF and RF-to-RF synchronization limit.

INTRODUCTION

Due to fundamental and applied experimental requirements, LLRF accelerator systems demand high levels of stability, accuracy, reproducibility, and monitoring capability. Over the past two decades, the availability of FPGA boards and control electronics has been significantly improved. Today, it is possible to implement FPGA-based LLRF feedback and feedforward systems for precise control of the accelerating field using high-frequency ADC and DAC boards (down-conversion technique). There are two options to incorporate feedback&feedforward into the LLRF system. The first option uses an external I/Q demodulator, FPGA board to digitize the I/Q signals, calculate the phase and amplitude corrections, apply feedback and feedforward algorithms, and external I/Q modulator to regenerate the RF signal. This method does not require an expensive, highly stable local oscillator or signal generator to down-convert signals received from the waveguide or RF cavity. The second option is similar, but the I/Q demodulator and modulator are implemented within the FPGA logic. Both approaches requires the implementation of a specific LLRF signal distribution architecture to synchronize the accelerating field phase with the RF-Gun laser pulse arrival time. This report introduces a new LLRF system architecture for the KEK LUCX facility [1, 2] and discusses the facility's phase stabilization limit.

LLRF SYSTEM ARCHITECTURES OVERVIEW

To date, several LLRF system architectures were implemented at accelerator facilities. Nevertheless, these architectures implementation approaches can be joined into 2 big groups. The first group utilizes a Signal Generator (SG) with external phase shifter and amplitude modulator modules of different form-factors such as NIM or VME. The phase shift and amplitude modulation are controlled by a controller with DACs. Sometimes, I/Q modulator modules is implemented to shift the accelerating field phase.

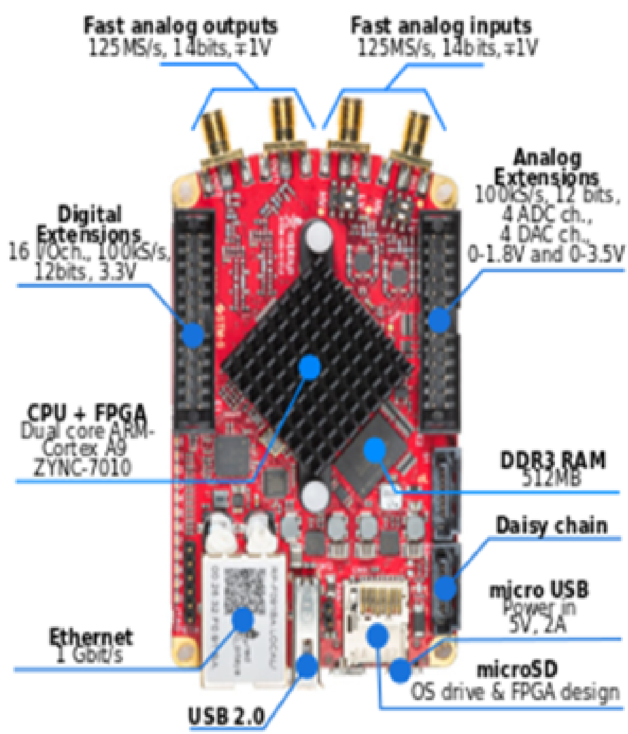

Figure 1: RedPitaya STEMlab 125-14 FPGA board overview.

The second group is based on a FPGA board equipped with System on Chip (SoC) and Phase-Locked Loop (PLL), which accepts an external reference signal from Master SG [3, 4]. The master SG generates the accelerating frequency signal, which is divided several times to get the lower frequency subharmonic. Moreover, this architecture key point is a Slave SG. It is utilized to generate the Local

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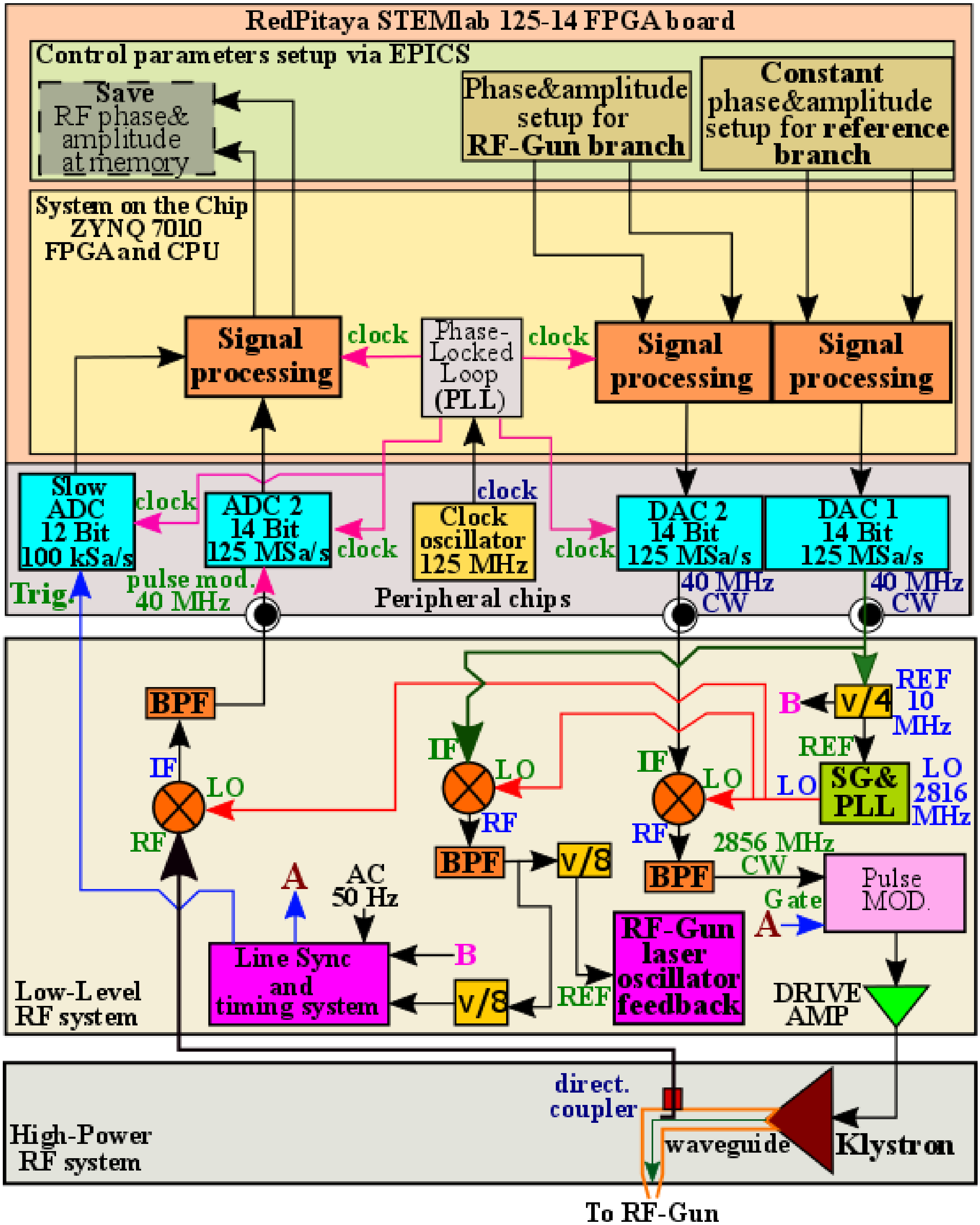

Figure 2: Simplified schematic of KEK LUCX facility RF-Gun LLRF system branch with RedPitaya STEMlab 125-14 FPGA board based LLRF phase&amplitude control.

Oscillator (LO) signal for frequency down-conversion and up-conversion. Master ans Slave SGs are synchronized to each-other via preinstalled conventional 10 MHz PLL.

The SGs phase stability level is 10s fs (RMS), which does not degrade the phase stability of up-converted and down-converted signals. Frequency up-conversion and down-conversion is based on LO signal mixing with Intermediate

Frequency (IF) signal generated by FPGA board DAC output in the RF-Mixer.

It was decided to use the advantages of the both groups to develop new architecture and implement it at KEK LUCX facility. LUCX accelerator approach consists on a commercially available FPGA board and only one SG with preinstalled conventional 10 MHz PLL. The FPGA board is considered as Master, while the SG generates the LO signal for frequency up- and down-conversion.

KEK LUCX FACILITY NEW LLRF SYSTEM

KEK LUCX facility LLRF system setup consists of Red-Pitaya STEMlab 125-14 FPGA board [5, 6] (see Fig. 1), frequency dividers, Agilent E8663B SG with preinstalled conventional 10 MHz PLL, RF-mixers, band-pass filters (BPF) and pulse modulator. The LLRF system schematics is demonstrated on the Fig. 2. The FPGA board periphery is equipped with two channel DC-coupled 14 bit ADC, two channel DC-coupled 14 bit DAC both with 125 MSa/s sampling rate and additional 12 bit ADC with 100 kSa/s sampling rate. The internal oscillator generates the clock for the periphery and signal processing logic. The DAC 1 output is utilized to phase-lock the FPGA board with SG using conventional preinstalled 10 MHz PLL. The DAC 1 output generates the 40 MHz sine wave (CW) signal constant phase and amplitude. The signal is divided into two branches. Then, the first branch signal frequency is divided by 4 and fed to the 10 MHz PLL input. The phase-locked SG generates 2816 MHz CW LO signal for frequency up- and down-conversion purposes. The second branch signal is fed to the RF-mixer IF input, while 2816 MHz CW is injected into the LO input. The mixer RF output is filtered by waveguide type narrow-band BPF to reject side-harmonics occurred during the signal mixing. The resulting frequency after filtering is 2856 MHz with constant phase and amplitude. On the next stage, the up-converted frequency is divided by 8 to get the 8th sub-harmonic of the accelerating frequency to phase-lock it with RF-Gun laser oscillator feedback and timing system. Moreover, the timing system is phase-locked to the 10 MHz reference signal by the Line Sync generator (Tsuji Denshi Co. Ltd). Also, the Line Sync is locked to AC line to eliminate 50 Hz AC line instability onto the LLRF system.

The DAC 2 output generates the 40 MHz CW signal, which is up-converted to 2856 MHz by mixing with the common LO. The RF output is filtered by the BPF. The resulting frequency phase and amplitude are controlled by DAC 2. Then, it is modulated by 3.125 Hz, 4 μs width gate signal generated by the LUCX timing system. On the final stage, the RF pusle is amplified up to 700 W by the drive amplifier (Nihon Koshuna) and supplied to the klystron (Toshiba 3729). The klystron amplifies RF power from 700 W to 12 MW, which is transferred to the 3.6-cell RF-Gun cavity via waveguide system. The RF field directed to the RF-Gun is picked up by the directional coupler installed at the waveguide. The directional coupler directivity and coupling are 20 dB and 60 dB, correspondingly. The picked up RF signal is down-converted from 2856 MHz to 40 MHz by mixing with the common LO and the resulting IF frequency is filtered by the BPF, digitized by ADC, processed by the signal processing logic to get phase and amplitude of the accelerating field. The phase and amplitude information is saved to the EPICS PV.

The KEK LUCX facility has 2 normal conductive standing-wave accelerating cavities, such as RF-Gun and 12-cell Linac, RF-Gun laser and Compton laser. The entire LLRF system has 2 FPGA boards, which are phase-locked with each-other via SATA cable. The Master board internal oscillator sends 125 MHz clock signal to the Slave board PLL via SATA cable. Master board controls RF-Gun accelerating field and its laser phase&amplitude, while Slave board controls 12-cell Linac accelerating field phase&amplitude and Compton laser oscillator piezo feedback.

CW SIGNALS PHASE STABILITY MEASUREMENT RESULTS

The maximum possible RF-Gun laser phase injection stability is defined by the 357 MHz and 2856 MHz CW signals phase stability. It was measured by Keysight SSA 5052B Signal Source Analyzer, which setup was tuned to get the best measurement performance. IF Gain and number of correlations were 50 dB and 10, correspondingly. The phase noise SSB was integrated from 10 Hz to 10 MHz frequency offset.

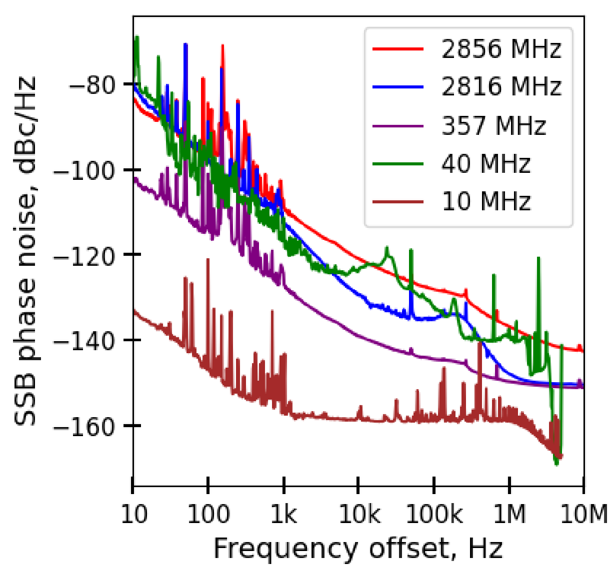

Figure 3: CW signals phase noise map.

As can be seen from the plot (see Fig. 3), the reference signal injected into the 10 MHz PLL phase noise is 0.005 ° (RMS). While, the IF signal noise is 0.03 ° (RMS). The LO and RF signals noises are 0.048 ° (RMS) and 0.079 ° (RMS), correspondingly. The accelerating field 8th sub-harmonic phase noise is 0.012 ° (RMS) or 92 fs (RMS).

CONCLUSION

KEK LUCX facility new LLRF system was developed for the precise control of the accelerating field phase and amplitude. The system is based on RedPitaya STEMlab 125-14 FPGA board and Agilent E8663B Analog Signal Generator with preinstalled conventional 10 MHz PLL. New LLRF system architecture allows to control RF-Gun laser injection phase with 100 fs (RMS) precision, while the stability of the RF-Gun accelerating field phase relative 12-cell Linac accelerating field phase is 120 fs (RMS). Moreover, the synchronization limit between the Compton laser pulses train and electron beam is also 100 fs (RMS), because the Compton laser cavity is synchronized to the 357 MHz CW reference signal. Nevertheless, RF-Gun, 12-cell Linac and Compton laser need the phase and amplitude feedback&feedforward to eliminate any drifts caused by temperature or humidity fluctuations in the accelerator tunnel. The feedback&feedforward system is currently tested at KEK LUCX facility.

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