RF CONTROL SYSTEM OF THE HIMAC SYNCHROTRON

M. Kanazawa, K. Sato, A. Itano, K. Noda, E. Takada
M. Sudo, T. Kouno, A. Kitagawa, H. Ogawa, Y. Sato
S. Yamada, T. Yamada, Y. Hirao
National Institute of Radiological Sciences, Acc. Res. Div
9-1, Anagawa-4-chome, Chiba-shi 260, Japan

M. Shigeta, N. Tsuzuki, C. Yamazaki, E. Toyoda, T. Yagi, Y. Morii
Toshiba Corporation, Fuchu Works
1, Toshiba-cho, Fuchu-shi, Tokyo, 183, Japan

Abstract

We have developed the RF control system of the HIMAC synchrotron. This system consists of the high sensitive beam monitors, the digital low level controller with the digital synthesizer, and the pattern memories with one board CPU. The simulator of the synchrotron oscillation has been also developed to test the $\Delta\Phi$ (phase difference between the beam and the acceleration voltage) feedback loop. This paper describes the control system, the simulator, and the tested result with the simulator.

Introduction

We have made an RF control system for HIMAC synchrotron. In building this system, we have developed a pattern memory device, a digital beam monitor with high signal-to-noise ratio (S/N) specifications, and low level electronics which uses a digital synthesizer. The HIMAC RF control system is shown in Fig. 1.

Further we developed a beam simulator. By using this simulator we can check the RF control functions without an accelerator. We confirmed that the RF control system can suppress synchrotron oscillation using this beam simulator. We can, therefore, test the feedback system at the manufacturing factory without needing large accelerator facilities.

In this paper we explain the beam acceleration control system and the beam simulator system, and report the corresponding experiment results.

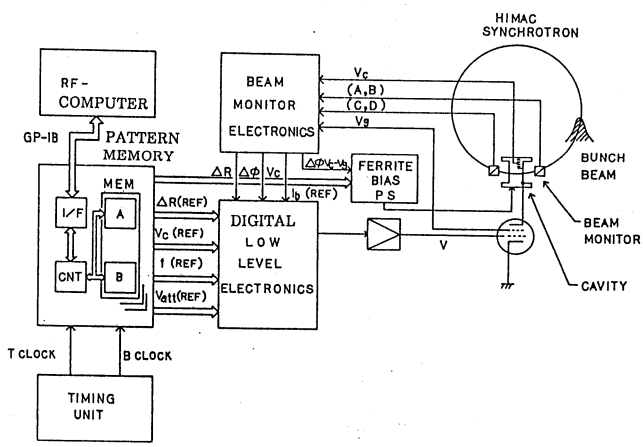

Fig. 1 RF control system of HIMAC synchrotron
I/F : GP-IB interface
MEM : Memory

RF Acceleration Control System

Pattern Memory Device

The pattern memory device is designed to control RF acceleration devices, and consists of CPU, GP-IB interface, power supply, and five pattern memory modules.

The pattern memory is connected to the RF computer through the GP-IB interface board. The RF computer transfers the pattern data and commands to the pattern memory by the GP-IB cable.

The CPU board receives the command and the pattern data, and writes the pattern data into the specified memory module. In short, it acts as the controller of the pattern memory.

Each memory module board has two memories. One is called A-memory, and the other is called B-memory. The memory channel (AorB) is selected by the memory change switch signal from the RF computer. When one memory is accessed to write data, the other memory outputs the control data. Each memory stores the control signal pattern and outputs the data to the external control devices synchronously with the clock signal from the external timing system. Each memory has the capacity to store 128 k words of data.

The timing system generates three types of clocks, which are called T clock, B+ clock and B− clock. T clock has a frequency less than 50 kHz. B+ clock is generated according to a 0.2 G increase of the magnetic field in the bending magnet. B− clock is generated according to a 0.2 G decrease of the magnetic field in the bending magnet. The maximum B clock frequency must be less than 120 KHz.

Table 1
The Specificatin of HIMAC Synchrotron

Contents	Typical Values
· Particle Species	^{4}He to ^{28}Si, ^{40}Ar
· Injection Energy	6Mev/u
· Energy Top	100~800 MeV/u for q/A=1/2
· RF Frequency Range	1~8 MHz
· Beam Intensity	10^{7}~10^{9} (He) ppp
· Repetition Rate	0.5 Hz at 600 MeV/u
· Acceleration time	<0.7s
· Momentum Spread	±0.3%

A word data has a 24 bit structure. The Most Significant Bit (MSB) is a parity bit that checks the parity of the word. The 4th bit to Least Significant Bit (LSB) constructs the main control pattern data. It is possible to set jump address a1 and a2 with a command from the RF computer. Jump address a1 contains data of the acceleration start point. Jump address a2 contains data of the flat top point. The pointer jumps to a1 by J1 event signal and jumps to a2 by J2 event signal that the timing system generates.

When the reset signal comes into the pattern memory from the timing system, the pointer is reset to the original point of the memory. When the memory module becomes abnormal, the module sends the abnormal signal to the RF computer.

Beam Monitor Electronics

The beam monitor electronics are shown in Fig. 2 and the specifications are summarized in Table 2.

The beam monitor consists of the following four parts : (1) Beam position monitor (ΔR) (2) Phase difference monitor between the beam and the acceleration voltage (ΔΦ) (3) Phase difference monitor between the acceleration voltage and the voltage of the grid (ΔΦVc−Vg) (4) Monitor to measure the acceleration voltage (Vc).

The features of the beam monitor electronics are :

(1) Noise Reduction

The beam signal is detected by the beam monitors which are installed both side of RF cavity, are summed up to reduce the RF noise with factor of 3.

(2) High-Precision Processing

In order to suppress the white noise we used the heterodyne method which increases S/N. Converting the frequency to 455 kHz, the calculation was executed.

Table 2
The Specification of Beam Monitor

Spec. / Monitor	Input Signal	Precision	Step Response
· ΔΦ Beam-Vc	Beam 70μV~100 mVp-p Vc 30mV~1 Vp-p	≦10% for ±180°	≦7μs
· ΔR	70μV~100 mVp-p	≦10% for ±100mm	≦18 μs
· ΔΦVc-Vg	Vc 10mV~1 Vp-p	≦10% for ±90°	≦20 μs
· Vc	10mV~1 Vp-p	≦2% for 5V	≦5 μs

(3) High-Speed Response Phase Detector

After the phase difference is coneverted to pulse width with the type ECL flip-flop circuit, the original wave with frequency 455 kHz is rejected. The high-frequency component waves are rejected by using a low pass filter. This results in low - noise and high - speed response phase difference detection.

RF Low Level Electronics

Fig. 3 shows a block diagram of the RF low level electronics (RF−LE). This system controls the frequency and amplitude. The design parameters of RF-LE are shown in Table 3.

The characteristics of RF-LE are :

(1) A digital direct-frequency synthesizer (STEL-1375A) with wide-band frequency and high-level accuracy

(2) Digital operated high - speed controllers can shut out electrical noise

(3) A high - speed frequency and amplitude switching cycle

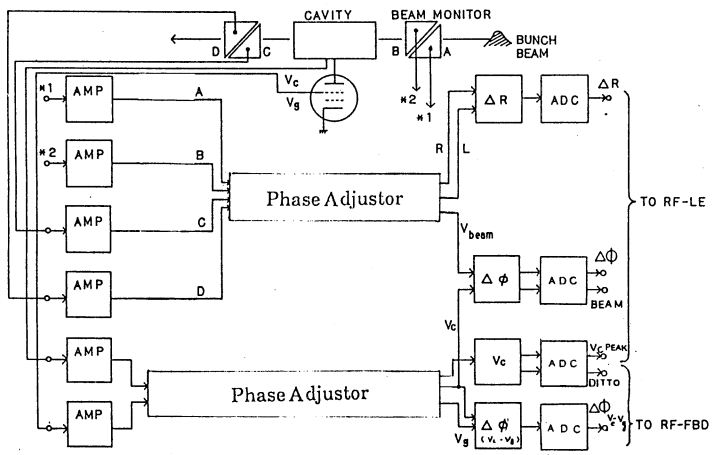

Fig. 2 Beam monitor electronics

Vc : Acceleration voltage
Vg : Control grid voltage
ΔR : ΔR processor
ΔΦ : ΔΦ processor
Vc : Vc detector
ΔΦ (Vc-Vg): ΔΦ (Vc-Vg) processor
ADC : A / D convertor

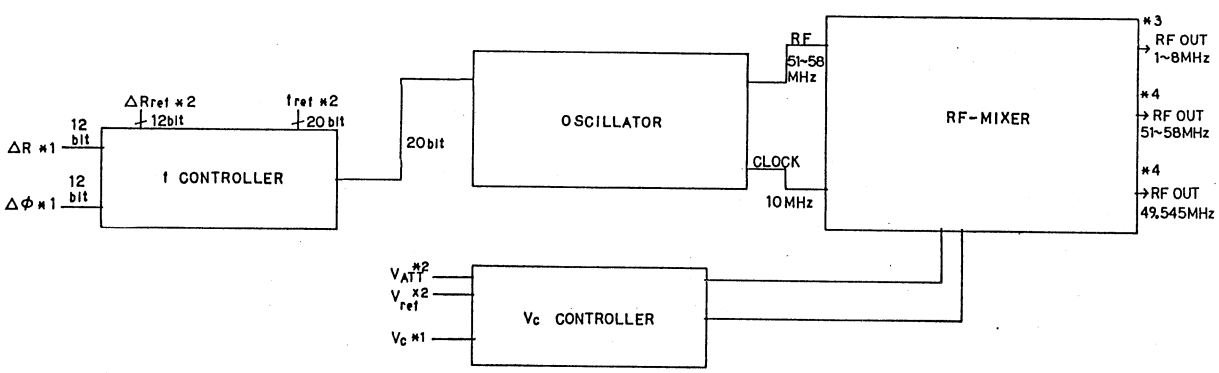

Fig. 3 RF low level electronics

*1 : From beam monitor electronics
*2 : From pattern memory device
*3 : For RF power amplifier (cavity)
*4 : For beam monitor electronics

The f controller executes the frequency feedback controls with ΔR and $\Delta\Phi$ data. After these controls, the corrected frequency data is output to the oscillator. The oscillator outputs the RF signal with this corrected frequency data.

The Vc controller compares the reference of the cavity voltage Vc (ref) with the measured value Vc and inputs the amplitude data to the RF mixer.

The RF mixer mixes the corrected amplitude with the corrected frequency and outputs the RF acceleration signal with a frequency of $1 \sim 8$ MHz and amplitude of $-23 \sim 20$ dBm.

Fig. 4 shows the frequency switching characteristics of the oscillator. As shown in this figure, the frequency changing time is about 1.2 μs.

Beam Simulator Test

The HIMAC RF system includes the following feedback control loops : (1) automatic voltage control loop, (2) automatic cavity tuning control loop, (3) longitudinal phase oscillation ($\Delta\Phi$) suppression loop, and (4) radial beam position (ΔR) control loop. The former two can be tested at the manufacturing factory without beam test. The latter two, however, have always been tested under different circumstances, even in a restricted manner.

A simulator enabled us to test the dynamic characteristics of the $\Delta\Phi$ suppression loop without beam test. Fig. 5 shows a schematic diagram of our simulator test.

The construction of the simulator resembles a phase-locked loop (PLL), widely used for many RF applications. Notice that an integrator plays an essential role here ; it produces an additional 90° phase lag in the PLL loop. The total phase lag in the PLL loop adds up to more than 180°, together with another 90° lag which is attributed to the frequency-to-phase conversion process inherently included in every PLL loop. As feedback control theory shows, therefore, the output frequency of the VCO does not lock to the RF signal supplied to the RF port of a double balanced mixer (DBM), but continues fluctuating around the RF port signal frequency. Adjusting the fluctuation frequency to equal that of synchrotron oscillation constitutes a phase oscillator simulator. Thus, feedback of the VCO output signal to the low level controller through the $\Delta\Phi$ monitor device completes the loop. If the $\Delta\Phi$ feedback loop works as expected, the RF cavity voltage follows the "beam" oscillation and thus "synchrotron oscillation" in the PLL damps.

Table 3
The Specificatin of Low Level Electronics

Contents	Typical Values
· Accleration Frequency	1~8 MHz
· Main Oscillator	Digital Synthesizer
· Frequency Switching Cycle	2μs
· Stability and Accuracy of the Frequency Feedback Control	$\pm 1 \times 10^{-5}$
· Amplitude Control Dynamic Range	-23~20 dBm
· Amplitude Switching Cycle	2μs
· Harmonics	≦-25 dB (0~20 dBm)
· Linearlity	≦3% (0~20 dBm)

Fig. 6 shows a successful suppression of "synchrotron oscillation". This result proves that the dynamic behavior of the $\Delta\Phi$ control loop works as expected. This encouraged us to incorporate our control device into TARN2. This led to the early success in our beam acceleration test on TARN2.

Conclusion

We confirmed and obtained the pattern control techniques for the acceleration of heavy ion beams using the pattern memory device.

We have established the method to test the beam acceleration feedback system with the beam simulator at the manufacturing facility level. The experiment with this simulator confirmed that the functions of the RF acceleration control system are effective to accelerate the beam in HIMAC synchrotron.

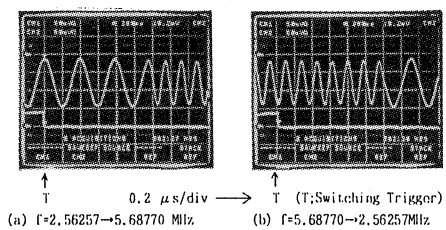

Fig.4 Frequency switching of the oscillator

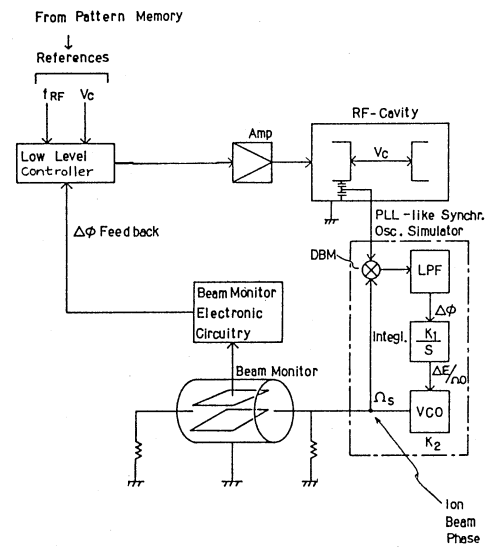

Fig. 5 Beam Simulator System
($\Delta\Phi$ Feedback Test)

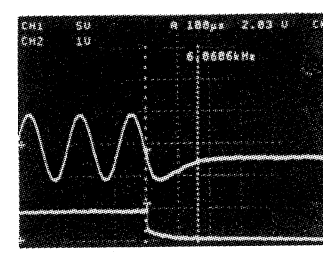

Fig. 6 Suppresion of synchrotron oscillation
Upper Curve : Synchrotron Oscillation
Lower Curve : $\Delta\Phi$ Feedback Control Signal