PA42

Analog Processor for Emittance Monitor in SPring-8 Linac

K.Yanagida, Y.Itoh, H.Yoshikawa, T.Hori, S.Suzuki, A.Mizuno, H.Sakaki,
T.Taniuchi, A.Kuba, T.Okada, M.Kodera and H.Yokomizo
JASRI-JAERI-RIKEN SPring-8 Project Team
SPring-8, Kamigori-cho, Ako-gun, Hyogo-ken, 678-12, Japan

Abstract

The analog processor for the emittance monitor in the SPring-8 linac is composed of a charge sensitive amplifier with gain control, a sample/hold circuit and an isolation circuit. The charge sensitive amplifier detects pulsed charge from the wire scanner. The sample/hold circuit maintains the signal to which can be accepted by an A/D converter on VME computer. It is designed as 1V/pC, 0.1V/pC or 1V/nC. The linear region was measured as -5V~5V of output. Fluctuation of output for 200 seconds was ~1.5mV of 1σ. However voltage drift was observed for 150 hours. But this is acceptable for emittance measurement.

1. Introduction

Profile monitors are generally used for emittance measurement. There are many kinds of profile monitors for example a wire scanner, a scintillation screen, an OTR monitor and so on. In the SPring-8 linac, a wire scanner is employed for the emittance monitor [1]. When an electron beam impinges on the wire, secondary emission charge and the bremsstrahlung are generated. Both are proportional to the charge of incident electron beam. An analog processor which detects the secondary emission charge is employed for the emittance monitor in the SPring-8 linac. However the efficiency of secondary emission charge from incident charge is reported as 6~7% for total surface at 30MeV~1GeV. Because of this low efficiency, a high gain charge sensitive amplifier is required. The analog processor has a sensitivity of 1V/pC nominally. The minimum charge is expected as ≤0.01pC/pulse at the positron mode (1ns width and 10mA peak current). Therefore the minimum signal output is expected as ≤10mV. The fluctuation of output signal is must be comparable (~10mV of 6σ) to measure the positron beam profile.

Because an A/D converter on VME computer only acquires DC voltage, the output signal of the charge sensitive amplifier is processed to DC voltage by a sample/hold circuit.

2. Composition of Analog Processor

The analog processor is mounted on a print circuit board (see Fig. 1). The main components are a charge sensitive amplifier (CS-507, CLEAR-PULSE), a sample/hold IC (AD1154, ANALOG DEVICES), an adjusting circuit and an isolation circuit. The block diagram is shown in Fig. 2.

Two diodes (PAD1, SILICONIX) are used for input protection. The PAD1 is a low leak diode which has specification of <1pA leak current. When the voltage exceeds over ±6V at the input of CS-507, the extra charge is bypassed though the diode.

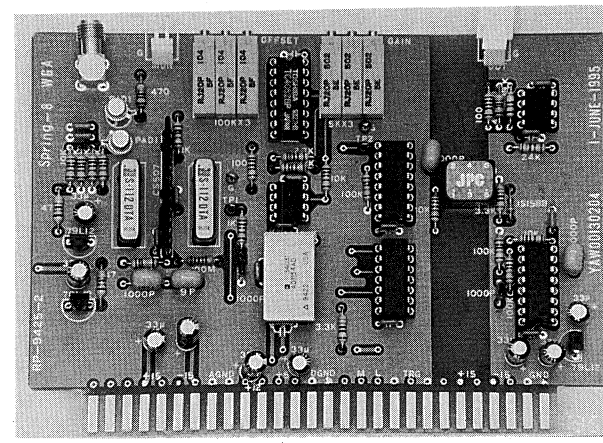

Fig. 1 Photograph of the analog processor.

The CS-507 is a hybrid IC which has a sensitivity of 1V/pC, nominally i.e. the built-in feedback capacitance C_f of 1pF. In order to release the charge on the feedback capacitor a resistance of 1000MΩ is also attached in parallel with the capacitor. The time constant of relaxation becomes 1ms. The sensitivity can be changed by attaching external feedback capacitors. The sensitivities are designed as 1V/pC (C_f~1pF, high gain mode), 0.1V/pC (C_f~10pF, medium gain mode) and 1V/nC (C_f~1000pF, low gain mode). Of course each time constant of relaxation is designed as ~1ms. The sensitivity can be changed by remote control. An MOS-FET is used as input stage in the CS-507. It has offset voltage of ~-0.5V nominally. Therefore the offset voltage appears on the CS-507 output.

The AD1154 works to make a DC voltage from the pulsed signal of the CS-507. The appropriate external trigger is required for sampling.

The adjusting circuit adjusts sensitivity to designed one and offset at the output of analog processor. The adjustable range is designed as 0.88~1.54. The reason for exceeding of 54% is to compensate the increase of feedback capacitance due to the stray capacitance. This stray capacitance will be a problem especially for the high gain mode.

The isolation circuit breaks the ground inductor loop. When the ground line is connected to the vacuum chamber by two or more route, a ground inductor loop is constructed. If the impedance of the loop is small, a ground current flows. A ground current degrades the S/N ratio. If a ground current of 10nA flows, a voltage of 10V (high gain mode) emerges on the DC output. In the SPring-8 linac there are two isolation points. One is in the analog processor and the other is an isolation amplifier in the A/D converter on VME computer. The isolation method in the analog processor is described below. The DC voltage from the AD1154 is converted to

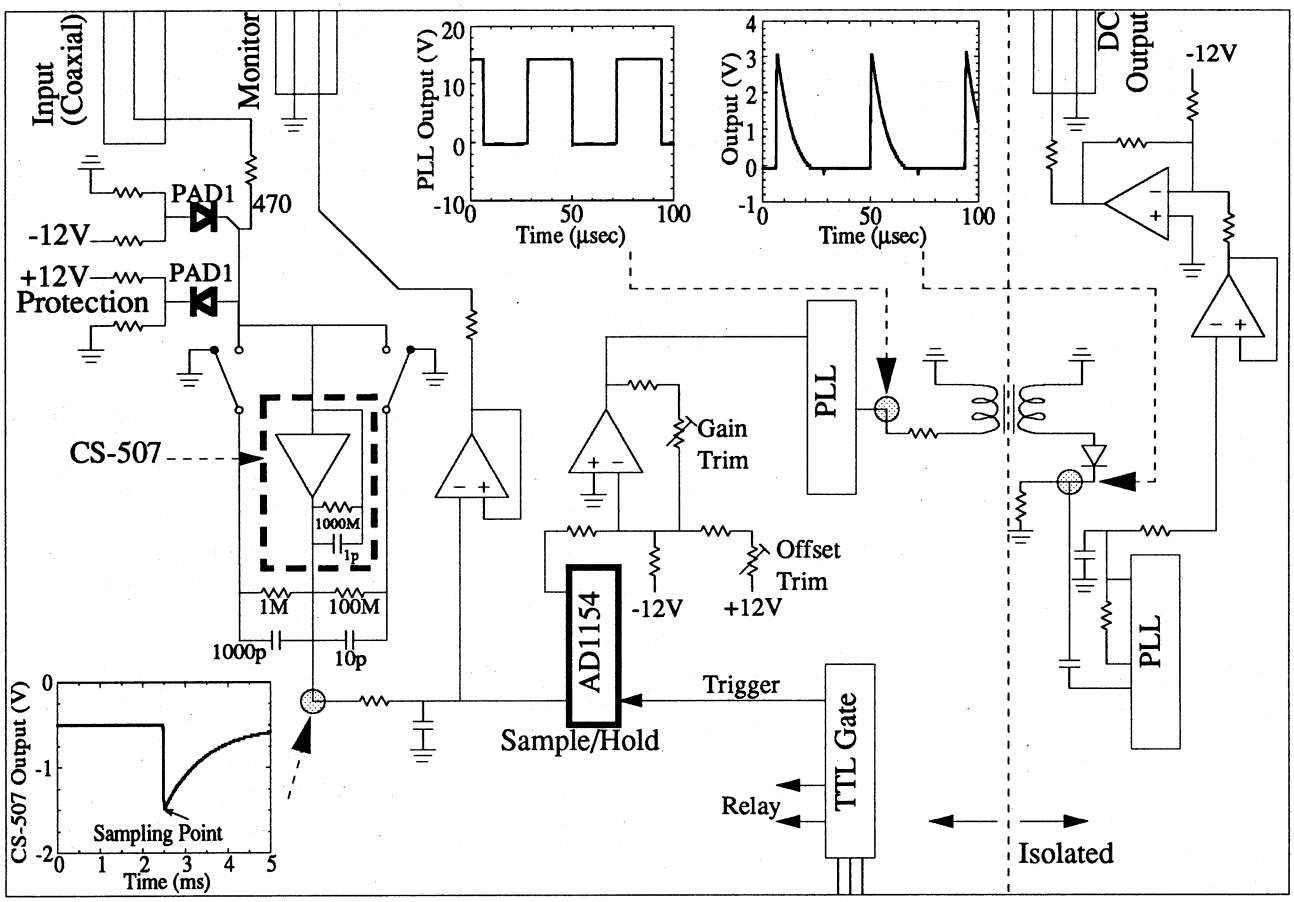

Fig. 2 Block diagram of analog processor.

frequency by the PLL circuit. Then the frequency is transferred through an isolation transformer to the second PLL circuit. Finally the frequency is restored to a DC voltage by the second PLL circuit.

3. Examination of Analog Processor

The analog processor was adjusted and examined using a simulated pulse. An appropriate reference capacitor C_i, 10pF, 100pF or 0.01μF, was connected to the input of the analog processor. When a step voltage V_i was applied, a corresponding charge $-C_iV_i$ was generated on the reference capacitor. At the same time the charge flowed into the analog processor. This means the charge of C_iV_i was transferred to the feedback capacitor of the charge sensitive amplifier. Fig. 3 shows the CS-507 outputs when various charges were applied. Due to the charge C_iV_i on the feedback capacitor, the CS-507 generated the voltage of $\frac{C_iV_i}{C_f}$. However the charge was released exponentially through the resister. Once the exponential curve was obtained, the peak voltage would be calculated by the curve fitting as the value at t=0. Fig. 4, Fig. 5 and Fig. 6 show the peak voltage of CS-507 output when the various charges were applied. The variation of DC output is also plotted. The region where the output is proportional to the input within ±1% is named linear region. The linear region was measured as -5V~+5V of DC output. The linear region will be extended to -10V~+5V of DC output if further adjustment will be performed. The sensitivity and the offset voltage are calculated by the curve fitting in the linear region. These measured characteristics are summarized in Table 1.

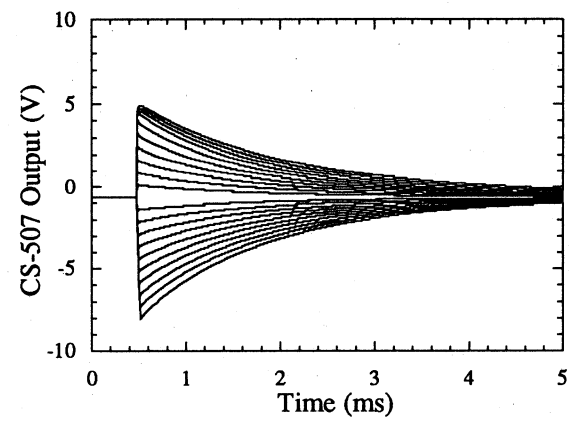

Fig. 3 CS-507 output when the simulated charge is applied from -10pC to 10pC by 1pC step.

The fluctuation (standard deviation) of DC output for 200 second (100 samples) was measured as shown in Fig. 7. The correlation between the input charge and the standard deviation means that this fluctuation was caused by the PLL circuit. The average is ~1.5mV (1σ).

This value can be acceptable to measure the positron beam profile.

Fig. 8 shows the fluctuation for 150 hours. Each data was acquired in different run. The maximum difference of CS-507 output is ~3.5mV. On the other hand the maximum difference of DC output is ~85mV. The sample/hold circuit and the isolation circuit may be affected by room temperature drift.

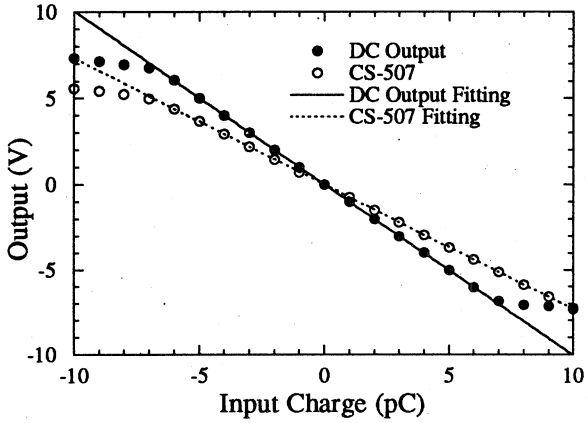

Fig. 4 Linearity curves of high gain mode for CS-507 output and DC output.

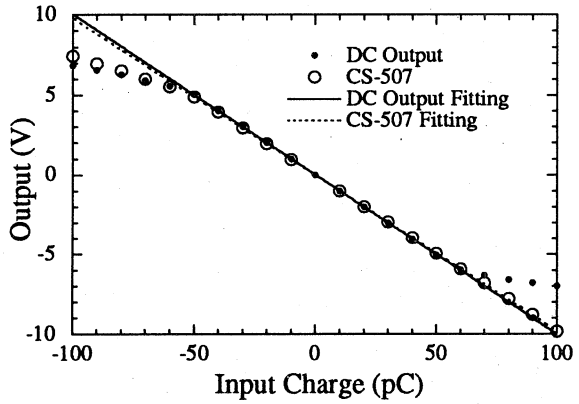

Fig. 5 Linearity curves of medium gain mode for CS-507 output and DC output.

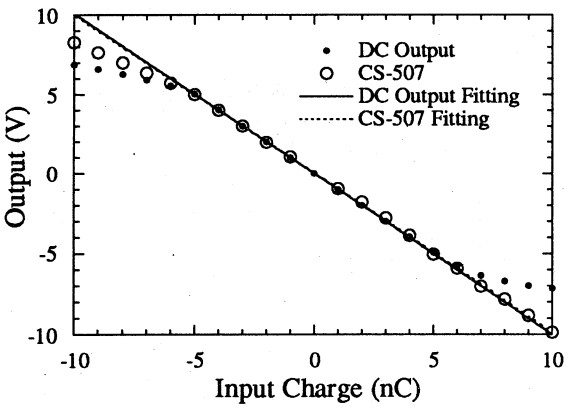

Fig. 6 Linearity curves of low gain mode for CS-507 output and DC output.

4. Conclusion

The analog processor achieved as designed characteristics. The fluctuation for 200 second can be acceptable to measure the positron beam profile. However the fluctuation for 150 hours is rather large. This means that measurement must be performed in few minutes. The linear region is -5V~+5V of DC output. This can be extended to -5V~+10V.

5. Reference

[1] K.Yanagida, et al., "Emittance Monitor for SPring-8 Linac." in Proc. of 1994 Linear Acc. Conf., Tsukuba, Japan, Aug. 1994, pp. 920-922.

Table 1
Measured data of sensitivity, offset and linearity

Output Gain	Linear Region	Sensitivity	Offset of DC Output
CS-507 High	-6~+10 [pC]	-0.7324 [V/pC]	NA
DC Output High	-6~+6 [pC]	-1.0046 [V/pC]	10.1 [mV]
CS-507 Medium	-50~+100 [pC]	-0.09795 [V/pC]	NA
DC Output Medium	-50~+60 [pC]	-0.10030 [V/pC]	6.35 [mV]
CS-507 Low	-5~+10 [nC]	-0.9920 [V/nC]	NA
DC Output Low	-5~+5 [nC]	-1.0038 [V/nC]	13.55 [mV]

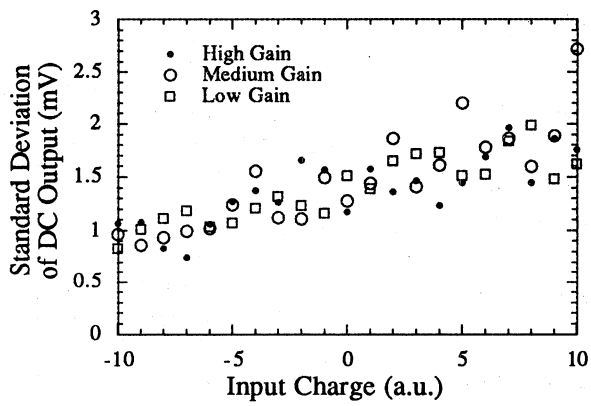

Fig. 7 Standard deviation of DC output.

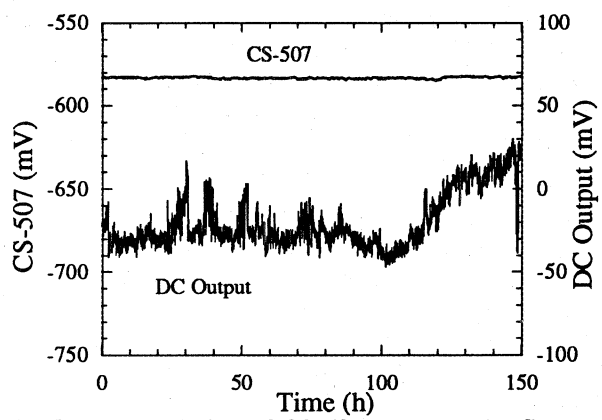

Fig. 8 Time evolution of CS-507 output and DC output for 150 hours.