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Development of a Two-Tap FIR Filter for Bunch-by-Bunch Feedback Systems

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Abstract

Simple digital filter system for bunch-by-bunch feedback systems have been developed. A two-tap FIR filter made of pure hardware system realizes the functions of the phase shift by 90°, the suppression of the static (DC) component and the digital delay of up to a hundred of turns. The difficulties in circuit board, such as the tuning of the time skews or the problem of the long-time reliability, have been solved by the development of custom GaAs LSIs which demultiplex and multiplex the fast digital data coming from ADC. The board has the size of 366.71×460 mm and is controlled through a VME interface. An application of the filter board, the transient memory recorder with 40 Mbytes of memory, enables us to analyze the oscillation modes of a multibunch beam with enough time span.

I. Introduction

For a storage ring which accumulate many bunches with high beam current, such as KEKB or PEP-II, it is very likely that it occurs many strong coupled bunch instabilities both in transverse and longitudinal planes. The methods to analyze and suppress these instabilities have the key to achieve the designed quality of the accelerators.

As the reduction of the sources of impedance, the strongest one comes from the higher order modes in the RF cavities, is essential to suppress the instabilities, some kind of special cavities to make impedance of higher order modes very low will be employed[1],[2],[3]. However, even with these cavities, impedance of some dangerous modes may remain high. Because of the many bunches with small bunch spacing, the frequency view of the instabilities will be complicated and spread over wide frequency range. To cure those unexpected instabilities, we are now developing beam feedback systems with the bunch-by-bunch scheme[4].

In the bunch-by-bunch feedback system, we detect the individual bunch oscillations separately, shift the phase of the signal by 90°, then kick the beam to damp the oscillation. In this paper we describe the digital filter system developed for KEKB rings which realize the functions of phase shift of any desired value, DC suppression and adjustable digital time delay. Related parameters of the KEKB accelerators are listed in Table I and are used without further explanations.

II. Selection of the filter

As the longitudinal front-end detects the position of a bunch in our case, it is necessary to shift the phase of the signal by 90° with the filter. The static (DC) component of a position signal, which will be a function of the relative position from the head of a bunch train, has no meaning and should be rejected from the feedback signal because it spends expensive feedback power in vainly. As the speed of a signal in a circuit or in a cable is far slower than that of a beam, feedback signals must wait the bunch re-arrival at the kicker after about one revolution of the bunch.

Ring		LER	HER	
Energy	E	3.5	8	GeV
Circumference	C	3016.26		m
Beam current	I	2.6	1.1	A
RF frequency	f_{RF}	508.887		MHz
Harmonic number	h	5120		
Particles/bunch	N	3.3×10^{10}	1.4×10^{10}	
Synchrotron tune	ν_s	$0.01 \sim 0.02$		

Table I
Main parameters of KEKB.

The great progress in the digital circuit technology, such as the speedy evolution of the digital signal processor (DSP), enables us to design complicated digital filter with considerable speed. It is completely programmable and has amazing flexibility. We can change the code dynamically even in the operation period without spoiling the function of the filter. Nevertheless, the present processor is not capable to handle the signal from the ADC alone. Demultiplexing and parallel processing with many DSPs is necessary. Moreover, in many cases we should employ the down sampling technique[5] to reduce the number of the DSPs.

Another approach, which we will employ for KEKB rings, is to make the simplest digital filter with the fast hardware logic circuits without down sampling technique. F. Pedersen of CERN has proposed the hardware two-tap FIR scheme for the filter[6]. As shown in Fig. 1, it has only two taps (-1) and $(+1)$ at $-270°$ and $-90°$ of the oscillation. The frequency response has peaks at f_s, $3f_s$, $\cdots$ and has zeros at 0, $2f_s$, $\cdots$. The passband around f_s is wide. We expect no filtering effect for noise component but for the DC. It is not a problem because we have measured the S/N of the detected signal from the ring and found very low noise components. The phase shift and

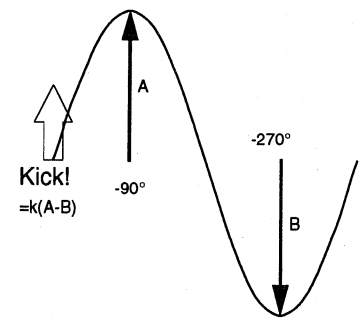

Figure. 1. Tap positions for the 2-Tap FIR filter.

the time delay are tunable with the selection of the tap positions with keeping the time between the two taps.

The difficulties of the filter lie on the complication of the high-frequency digital circuits. It accesses memories three times (one write and two reads) within one data period, in our case, 2 ns. This access speed is completely unreachable without demultiplexing the digital data in many parallel lines. Demultiplexing part is a fairly complicated circuit which needs very skilled treatments on the design and tuning of the time skews of many lines and the selection of the chips with same characteristics. The difficulty in the final multiplexing process is also a severe problem. The reliability of the board will be fairly doubtful. Making this filter with the combination of existing products seems to be impossible.

The difficulties have been solved by the development of custom LSIs to demultiplex and multiplex fast digital data. The small chips contain high speed circuits which would occupy large area with skilled treatments on the board. This maintenance-free chips enable us to use dense memories of CMOS technology and ensures high reliability for the board.

III. Custom LSIs

The circuit design and fabrication of the custom LSIs for the fast data demultiplexer (FDMUX) and the fast data multiplexe (FMUX) was made by Oki Electric Industry Co. Ltd. Table II shows the main specifications of the LSIs.

	FDMUX	FMUX
Technology	0.5μm GaAs DCFL	
Function	1:16 × 4bit	16:1× 4bit
Integration	~1.5k gates	~ 1.7k gates
Max. Clock freq.	> 700MHz	
Supply voltage	3.3V and 2.0V	
I/O	PECL and Lv-TTL	
Power consump.	2.5W	1.7W
Packaging	136pins ceramic QFP	

Table II
Main specifications for FDMUX and FMUX.

A. FDMUX

FDMUX demultiplexs 4 bits pseudo-ECL (PECL) signal up to 700 MHz to 16 channels × 4 bits of Lv-TTL signal. Here, PECL means the signal level of shifted by +2 V from the ordinary ECL level and the Lv-TTL means the reduced high level (3.3 V) TTL signal. By combining the two FDMUXs, we can create a 1:16 demultiplexer of 8 bits easily using the built-in synchronizer. The timing signal is also used to synchronize the FDMUX and the FMUX. All 16 channels 8 bits data are output simultaneously. It also offers two kinds of basic timing signals of Lv-TTL for the use of the downstream circuits. These basic timing signals will be useful and enough for many applications.

B. FMUX

FMUX multiplexes 16 channels × 4 bits of Lv-TTL signal to 4 bits PECL signal. Same as FDMUX, we can use 16:1 multiplexer with 8bits. It offes teh basic timing signals of Lv-TTL and PECL levels.

Figure 2 shows the bottom view of the FDMUX (GHDK4211) and FMUX (GHDK4212) chip.

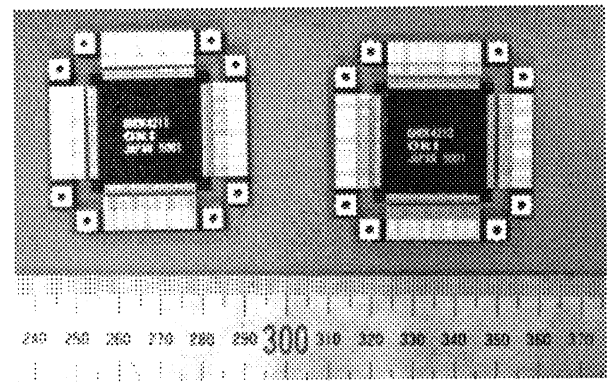

Figure. 2. Bottom view of FDMUX (GHDK4211) and FMUX (GHDK4212)

IV. Design of the filter board

Figure 3 shows the block diagram of the filter board. The size of the mother board is 366.71 mm×460 mm, where prior size corresponds to the triple height board of the VME bus. On the mother board, there are FDMUXs, FMUXs, a DAC, field programmable gate array (FPGA) chips for the address control. There are 16 slots of connectors on the board for the memory/subtracter daughter board. An ADC is also mounted on another daughter board.

A. ADC and DAC

We have a few candidates for the ADC which works under system clock of 508 MHz and has a enough analog bandwidth. We adopted a MAX101 of MAXIM, which works 500 MSPS with an 8 bit accuracy and have 1.1 GHz of analog bandwidth. It has a 1:2 demultiplexer in the chip so there are 2 channels of outputs.

We have more candidates of DAC for our purpose. We have chosen a TQ6122-M of TriQuint which works up to 1 GHz with an 8 bit accuracy and have a 2:1 multiplexer in the chip.

Because of the demultiplexer in MAX101, we will use 4 FDMUXs and 4 FMUXs on the board. The output of the ADC are therefore demultiplexed with 32 channels. The system clock (255 MHz) for upper 16 channels (A) and lower 16 channels (B) are supplied from the ADC. Each 16 channel works simultaneously.

B. Memory and ALU daughter board

Each channel handles 160 bunches for the case of KEKB rings. We use two sets of ring memories (A and B) per each channel to reduce the memory access from three (one write and two read) to two (one write and one read). Data from FDMUX is written in both memories in the same address simultaneously. In the next step, we read $-90°$ data from memory A, $-270°$ data from memory B in the same timing with different memory address. Because the time period of the data output from FDMUXs are about 64 ns, the use of CMOS SRAM with access speed ($\overline{WE}$) of 12 ns ensures us enough time margin. As it is necessary to

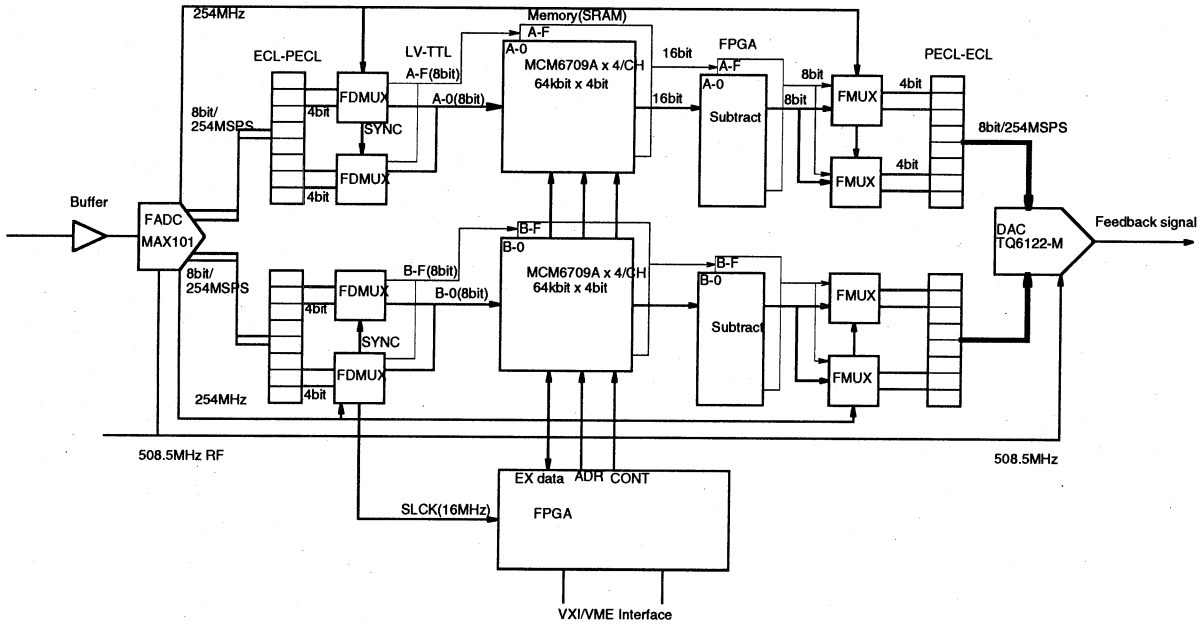

Figure. 3. Block diagram of the filter board. It has 4 FDMUXs and 4 FMUXs.

accumulate at least 100 turns of revolutions per a bunch, total memories needed amounts to 5120×100×2 bytes.

We use a FPGA with the function of an subtractor. It also contains a bit-shift mechanism that shifts the output of the subtractor from 0 to 3 bit upward. It enables us to change the gain of the filter up to 20 dB dynamically.

C. Address controller and interface

We must control three addresses pointers for memory access. One is the write address (WAB) that works 508.8 MHz/32=16 MHz. Other two addresses are used to point the 90° (RA) and 270° (RB) previous data for the bunch to feedback. We can set the address shifts of (RB-RA) and (WAB-RA) through a VME interface. Needless to say, the value must be multiples of 160 for the correct feedback. The difference between WAB and RA should be selected to tune the time delay of the feedback signal so as to have a maximum gain. We can change the time delay with the 2 ns step.

This board is now under fabrication and will be completed by the end of the September, 1995 and will be tested under the operation at TRISTAN-AR.

V. Application to beam-dynamics studies

The mother board is capable to the application of a transient memory recorder by replacing the memory/subtractor daughter board with a dense memory board and by replacing the address control FPGAs. In our design, the maximum memory we can mount on the board will be about 40 MB. For the KEKB rings, it will accumulate 8192 turns of bunch positions for all 5120 bunches. Combining the memory board and the feedback system enables us to measure the growth of the instability very clearly. This memory board will be completed by the end of 1995.

VI. Summary

For the circular accelerators that accumulate many bunches with fairly high beam current, the bunch-by-bunch feedback system will play a great role in the suppression and in the analysis of the instabilities. On the development of the bunch-by-bunch feedback system, however, there lie many difficulties concerning to the bandwidth of the system. In KEKB rings, the use of the custom LSIs for demultiplexing and multiplexing the digital data enables us to develop the pure hardware two-tap FIR filter system without downsampling technique, on one board of tirple-hight of VME. We expect that the board has good reliability because of the packaged high frequency circuits in the LISs. The feasibility of the board will be tested with the feedback experiment at TRISTAN-AR in these years.

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