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HIGH ACCURATE TIMING SYSTEM FOR THE SPRING-8 SYNCHROTRON

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Abstract

For the single bunch mode operation, the timing system for SPring-8 synchrotron is required high accuracy (low jitter) and high resolution. Prior to the timing system for SPring-8, we made a test timing system as a prototype. It achieved target specifications (jitter a. 20ps, resolution a. 20ps). In this paper, we'll report about the construction and some acquired data of the test timing system.

1. Introduction

SPring-8 has a "single bunch mode". In the single bunch mode, the injector (linac and synchrotron) injects 8 beam pulses into the storage ring. To make a single bunch, the beam pulse #2-#8 have to be injected at the timing when the bucket (which the beam pulse #1 is in) comes to the injection position of the storage ring.

The storage ring has 2436 buckets and the synchrotron has 672. So, the bunch in the synchrotron rounds 3 and 5/8 turns in the time the bunch in the storage ring rounds 1 turn. It means that for the effective single bunch injection, 8 beam bunchs have to exist in interval of 84 buckets (1/8 of 672) in the synchrotron. (Fig.1)

2. Requirement for the timing system

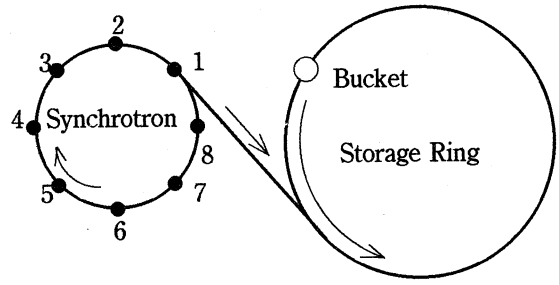
For this single bunch mode operation, following conditions are required.

(1) RF phase of the synchrotron and the storage ring are synchronized.

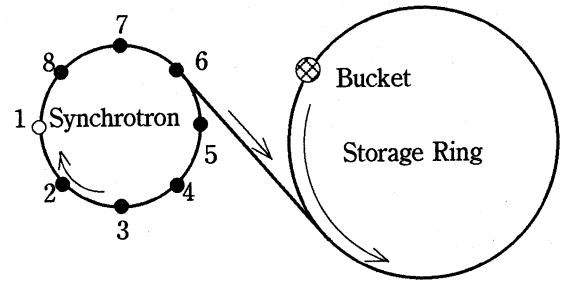
(2) Eight bunchs in the synchrotron are located in same interval correctly.

The 1st requirement is achieved, because the rf signal of the synchrotron is provided by the storage ring system. The 2nd one is satisfied if beam extracted from the linac is injected into the designed bucket in the synchrotron. The pulse length of the beam from the linac is 1nsec and the length of the bucket in the synchrotron is approximately 2nsec. (It's equal to the wave length of rf (=508.58MHz).)

So, the injection timing (from the linac ro the synchrotron) has to be adjustable in 100psec order timing with accuracy around 1/10 of the bucket length (2nsec).



a) Bunch #1 is injected to Storage Ring.



b) Bunch #6 is injected when the bunch come to the injection point. Thus, 8 bunchs are injected to the same bucket. The order will be bunch #1, #6, #3, #8, #5, #2, #7, #4.

Fig.1 Single bunch injection

3. Construction of the test system

Prior to the product for SPring-8, the test timing system was constructed. Specifications are:

Input signal
- One-cycle signal (1Hz)
- Master clock (508.58MHz)
- Reset signal (1Hz)

Output signal
- Linac trigger signals (8 pulses)

Synchronized start pulse (for monitor)
Synchronized clock (for monitor)
Jitter :less than +/− 100psec
Resolution : 100psec
Function : Generate 8 linac trigger signals (from the linac to the synchrotron.) every 16.7msec triggered by 1−cycle signal. (16.7msec : Cycle of the linac extraction)

To adjust "linac trigger signals" with low jitter and high resolution is the target of this test system. Major components of this test systems are:

(1) Synchronize circuit

Make synchronized clock signals from external clock (508.58MHz) and one−cycle signal.

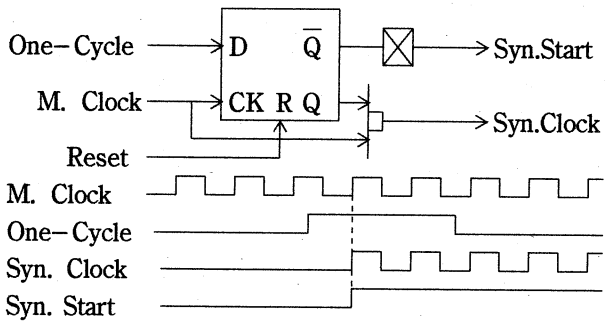


Fig.2 Synchronize circuit

(2) Counter circuit

(a) Bunch interval counter

Generate "bunch interval clock" every 84 synchronized clocks. 1 cycle of this clock (6.05MHz) is equal to the interval time of the bunch of the synchrotron in the single bunch mode.

(b) One−turn counter

Generate 8 signals which represent bunch number (#1−#8) which beam from linac will be injected into. This signals are rotated from #1 to #8 switched by "bunch interval clock". This signals are used in the logic circuit to make linac trigger signals. This counter has its own delay−line for its fine adjustment.

(c) Turn−number counter

(d) Injection−number counter

Both counters ((c) and (d)) are decreased by "bunch interval clocks". And they are also used in the logic circuit.

(3) Logic circuit

Generate 8 linac trigger signals. There are 8 logic circuits (#1−#8) and each logic circuit represents the order of linac trigger (#1−#8). To select logic circuit #1−#8, counter (b),(c) and (d) are used.

(4) Output circuit

Final sequence of the system. It generates 10nsec width pulses at the monomulti vibrator. It has a delay−line. Range of this delay−line is selected from 0.1nsec to 6.3nsec by 0.1nsec step. (It's selected by dipswitches.) The resolution of this system depends on this delay−line.

The feature of this timing system are:

(1) Frequency down converter isn't used, it minimizes jitter and gets fine resolution.

(2) One high speed counter (ECL element) and some cascade linked counters are used. These counters select the logic circuit and control the timing of the linac trigger pulse. This construction also minimizes jitter and high accuracy.

(3) A delay−line is used in the output circuit. This makes the adjustment of the delay timing easy.

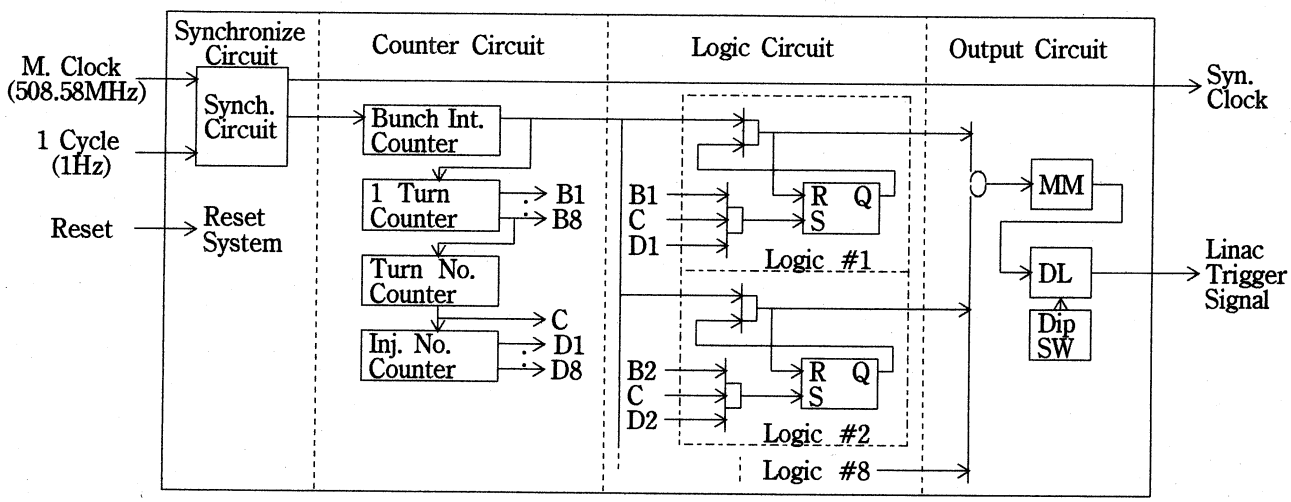


Fig.3 Construction of test timing system

4. Result of test system

To confirm reliability, miscounts were checked and jitter through the timing system was measured.

(1) Miscounts

The measurement system is shown in Fig.4. With a universal time−interval counter, time intervals between every linac trigger signals are measured. If there are N−times miscounts, time difference between maximum data and minimum data will be:

$$N \times (\text{cycle of clock}) = N \times (1/508.58\text{MHz}) = N \times 1.966\text{nsec}$$

Acquired data (Table 1) are less than 1.96nsec. It means there were not any miscounts.

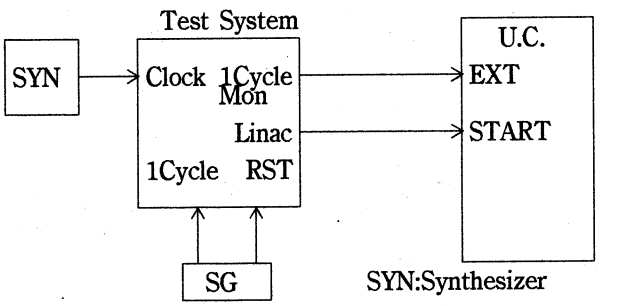


Fig.4 Measurement system for miscounts

Table 1 Data for miscount test

Signal	Tmax − Tmin
#1 − #2	0.45nsec
#2 − #3	0.49
#3 − #4	0.55
#4 − #5	0.45
#5 − #6	0.55
#6 − #7	0.53
#7 − #8	0.45

(2) Jitter

A measurement system is shown in Fig.5. A digital sampling oscilloscope is used for the measurement (connect "linac trigger signal" to the trigger channel and master clock (508.58MHz) to the channel for measurement).

Acquired data is shown in Fig.6. The width of the sine−curve represents jitter. Jitter is about 20psec after fine adjustment of the delay line, so this system satisfies the required specification for the single bunch mode operation.

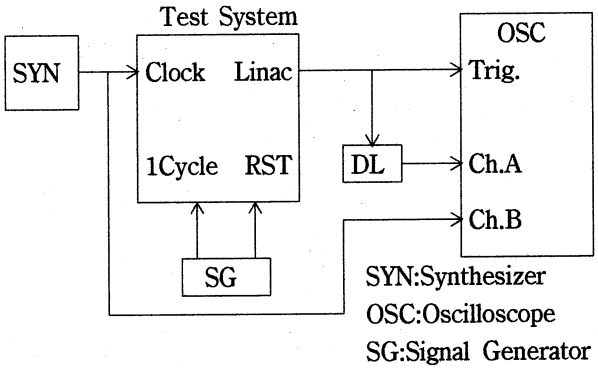


Fig.5 Measurement system for jitter

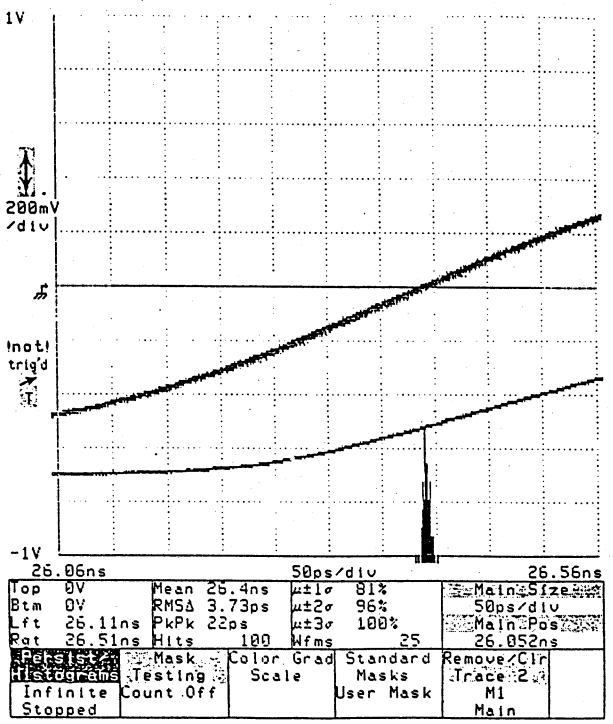


Fig.6 Acqired jitter data

5. Conclusion

The required specifications for timing system are achieved through the test system. The accuracy is around 20psec, and the resolution is less than 200psec. Now, the timing system for SPring−8 synchrotron are under manufacturing. The element for the delay−line in the output circuit will be changed in this machine. And this change will make the resolution higher up to 20psec.